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PORTABLE VAPOR SURVEILLANCE SYSTEM

by

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U. S. ARMY LAND WARFARE LABORATORY
Aberdeen Proving Ground, Maryland 21005

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20. ABSTRACT (*Continue on reverse side if necessary and identify by block number*)

A portable membrane separator-mass spectrometer vapor detection system has been developed. Components of the system are housed in two light weight aluminum suitcases. The system operates from commercial power lines and can be set up quickly and conveniently wherever 110 volt 60 Hz power is available. Internal operation is under microcomputer control with an operator's visual display showing computer processed data. The operator may select any of a number of modes and programs via switches which communicate with the computer.
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20. ABSTRACT CON'T

Although the microcomputer was developed specifically for this application, it is a true general purpose device with a full instruction set, direct memory addressing to 32K words and very extensive input-output capability. It thus can be applied with low cost to a variety of other applications.

FRONTISPIECE
The Portable Mass Spectrometer
Vapor Detection System

AD-782844

FOREWORD

The US Army Land Warfare Laboratory has sponsored a number of research and development efforts in the detection of targets by their chemical effluents. This work has been primarily directed toward the detection of vapors given off by concealed personnel, explosives and illicit drugs but is certainly applicable to other areas such as chemical warfare agents and industrial pollutants. The detection system discussed in this report is the culmination of a development cycle starting with a breadboard feasibility system in 1968. This system consists of a quadrupole mass spectrometer interfaced to the atmosphere with a Llewellyn membrane separator and controlled by a micro-computer. This is a truly portable system housed in two suitcase-size modules. This system may be operated as an aircraft or van-mounted system for plume intercept applications or may be used as a stationary checkpoint detector for searching vehicles or luggage for contraband or for detecting the presence of pollutants or chemical agents. Earlier systems under this task were developed by Varian Associates under Contract Nos. DAAD05-68-C-0335 and DAAD05-70-C-0197. Systems developed under these contracts have been operated and tested in both rotary and fixed-wing aircraft for airborne surveillance and in vans for ground surveillance.

This effort was sponsored by the US Army Land Warfare Laboratory, Advanced Development Division, Applied Physics Branch, under the technical supervision of Mr. H. Clay McDowell. The project was titled "Vapor Surveillance," LWL Task No. 03-P-68.

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FRONTISPIECE

I. INTRODUCTION

The U. S. Army Land Warfare Laboratory has sponsored work on several systems for vapor detection based on the Llewellyn separator - mass spectrometer instrument [1] and for application of these systems to various problems. [2] This report is concerned with the most recent work, sponsored under contract number DAAD-05-72-C-0253 which required the development and construction of two portable vapor detection systems.

Objectives of the development include the incorporation of performance features demonstrated in prior systems and packaging of all elements of the system in suitcases to facilitate transport without special requirement for packing, mounting and provisioning.

The delivery of the systems provides the user with a truly portable vapor detection capability with an on-line computer mediated control and display provision for quick investigation of trace vapor detection and analysis situations.

1. Contracts numbered DAAD-05-68-C-0335
   DAAD-05-70-C-0197
   DAAD-05-72-C-0091
2. Contracts numbered DAAD-05-71-C-0109
   DAAD-05-71-C-0110

II. GENERAL DESCRIPTION

The portable vapor detection system is housed in two 24 inch aluminum cases which are carried independently for transport. In operation, the cases are opened and interconnected. Power for operation is drawn from commercial lines at 110 volt, 60 HZ with an overall power consumption of approximately 300 watts. One rotary converter is furnished to operate the systems from vehicular power of 24 - 28 volts DC. Views of the system are shown in Figures 1 and 2. The cases housing the system are labeled A and B. Housed in case A are the control and display panel, the main power system, and the miniaturized general purpose digital computer. The quadrupole mass spectrometer, its vacuum system and analog drivers, its digital controller and detector system, and the membrane separators, along with power supplies and thermal controls are housed in case B. Three different sample inlet probes, each for a different sampling procedure, are provided for attachment when case B is opened.

In operation, with the two cases interconnected and powered, the system responds through switch commands to operator control. With mode and program selected, the operator may manipulate a sampling probe to explore the ambient trace vapor levels sought.

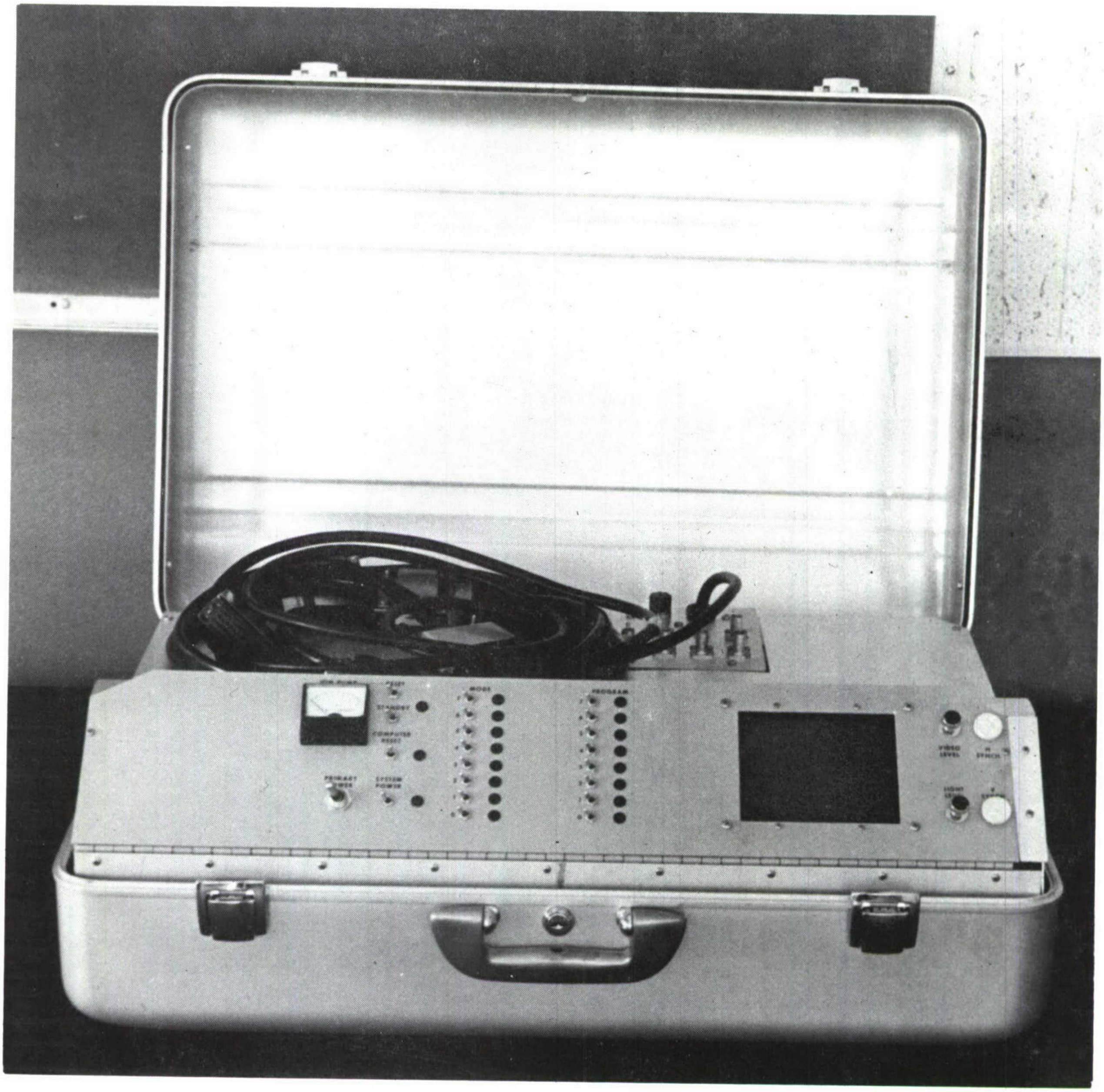


FIGURE 1
Operator Control and
Display Unit

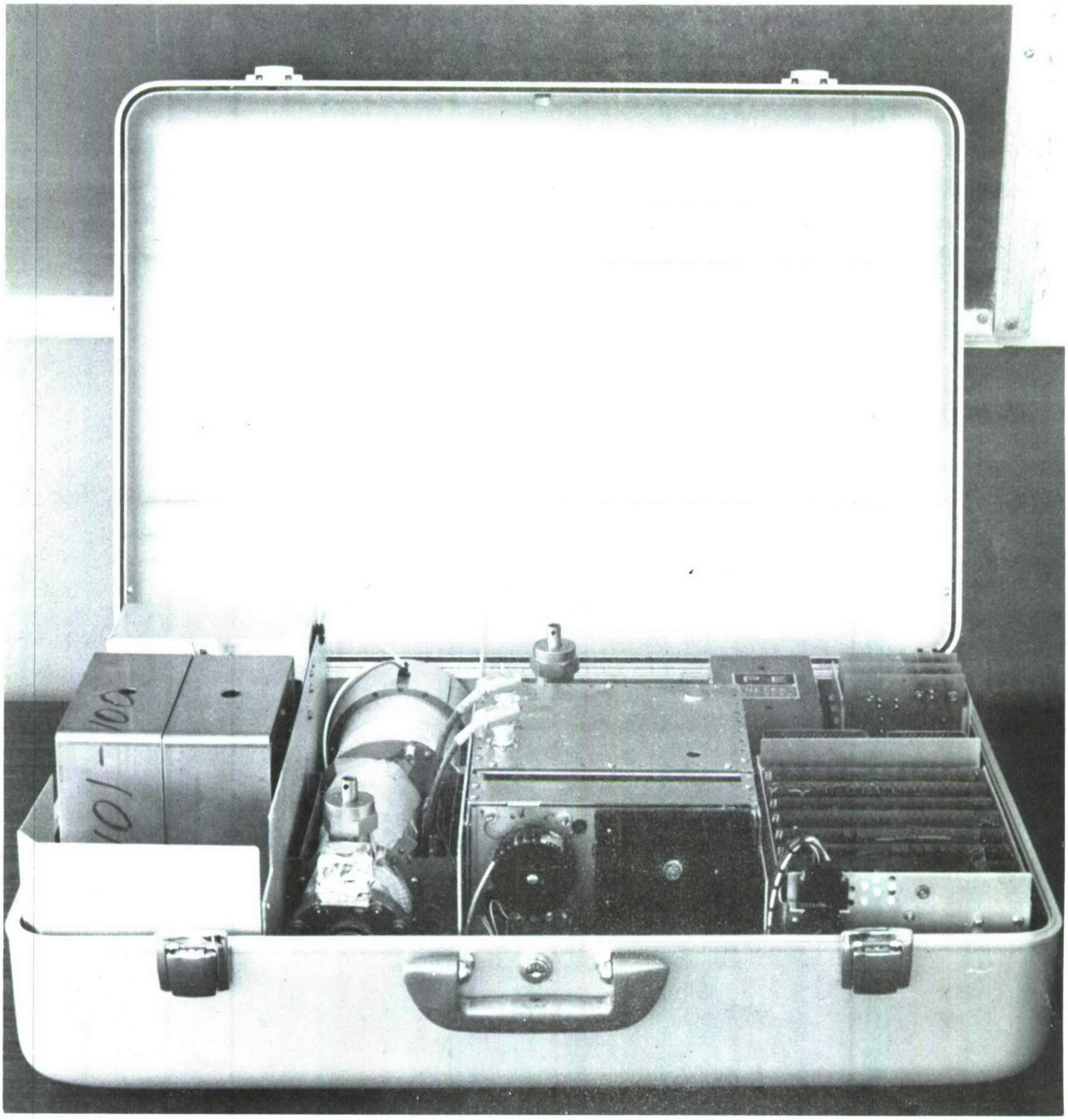


FIGURE 2
Mass Spectrometer Unit. Thermal
Insulation & Covers are Removed
In This Picture

Control of sampling includes judicious use of the air sample pump. Front panel switches allow retention of a detection display for study of a transient detection.

Since the computer memory includes a permanently programmed read only memory section, program protection is complete. Neither manipulation of panel switches or power outages can disable the stored program. Computer start up is automatically accomplished by the computer reset switch when system power is turned on, and shutdown occurs when power is turned off, no shutdown cycle or procedure being required.

The vacuum management of the system resembles that of units previously supplied.

High vacuum is maintained by an ion pump at normal pressures of 10^{-7} to 10^{-6} torr. A meter for monitoring the high vacuum is provided on the control panel. An adjustable vacuum interlock is connected to disable the quadrupole filament and rod supplies in the event of excessive pressure in the spectrometer. Power for the ion pump is supplied from the main power supply while the system is in operation. Provision is made for standby operation, using a direct current source at any voltage between 12 and 28 with current capability of less than 1 ampere (usually about 0.1 ampere). An alternating current adapter operating

from commercial power lines is furnished for standby operation. In addition, any suitable battery source may be used for transit purposes.

Separator interstage vacuum is maintained by two canisters of specially processed zeolite. Since the separator is continuously under ambient pressure at its inlet, there is a continual small entry of air gases into the interstage sinks even when the system is in a standby condition. Normally the interstage canisters are pumped down on a daily basis using a suitable fore pump. The normal pumpdown cycle requires approximately one hour and can be accomplished without operator attention except for pump connection and valve manipulation. Valves are provided on the system to accommodate sustained standby periods wherein daily pumping must be interrupted for more than 2 - 3 days. A relatively simple system pump down cycle is required after sustained standby periods.

The software provided in the read only memory of the computer accommodates a variety of operating modes. These include the observation of program selected mass peaks or blocks of the complete mass spectrum. Data are processed to generate filtered results and to supply comparisons with stored data from prior measurements or a slowly moving average value of mass

peak intensities. The operator may choose modes of operation most suitable to the measurements being made. While the read only memory program is nominally permanent, the memories can be removed from the system and reprogrammed very simply. This is of particular interest in the case of the section (one chip) containing the mass tables for programmed mass measurements. The use of reprogrammable read only memory chips for the remainder of the program (which would not normally be changed), provides a software flexibility to the system. Expansion capacity of more than a factor of two in read only memory is provided in the computer main frame.

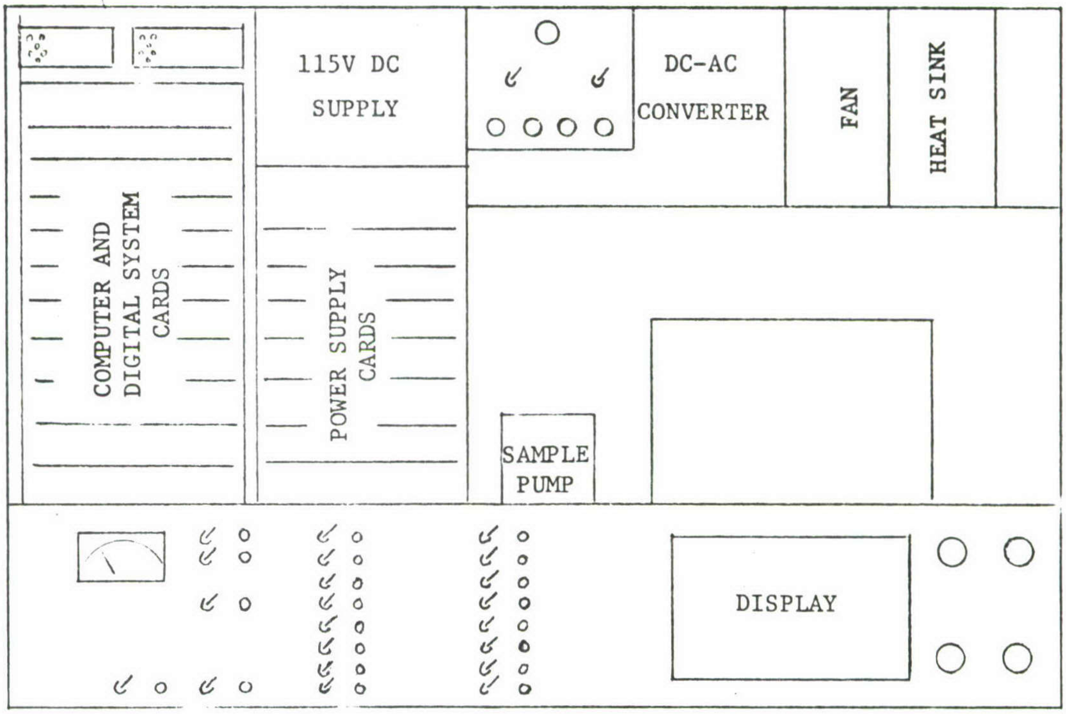
III. MECHANICAL HARDWARE

The portable vapor detection system compresses a considerable variety of components into the two cases. The requirement that normally bulky and delicate elements be fitted into portable cases placed several constraints on the design adopted. The mechanical distribution of parts of the system is schematically shown in Figure 3. Basic division of elements of the system between the two cases is such that the spectrometer, its vacuum system, separator and sample inlet, and its analog electrical components are housed in case B, while the computer, the control panel, the display, and the power system comprise the major elements housed in case A. The cases are required to support and protect the elements of the system against normal use and transportation hazards. Electronic elements pose no particular housing or support problems, being light weight and reasonably rugged. The spectrometer is mechanically vulnerable in two respects; namely, vacuum integrity, and alignment of internal parts.

A. FRAME AND CASE CONSTRUCTION

For support and housing of the system, cases fabricated by the Zero Manufacturing Company were selected. These cases are fabricated from deep drawn .051 inch high strength aluminum

CASE A



CASE B

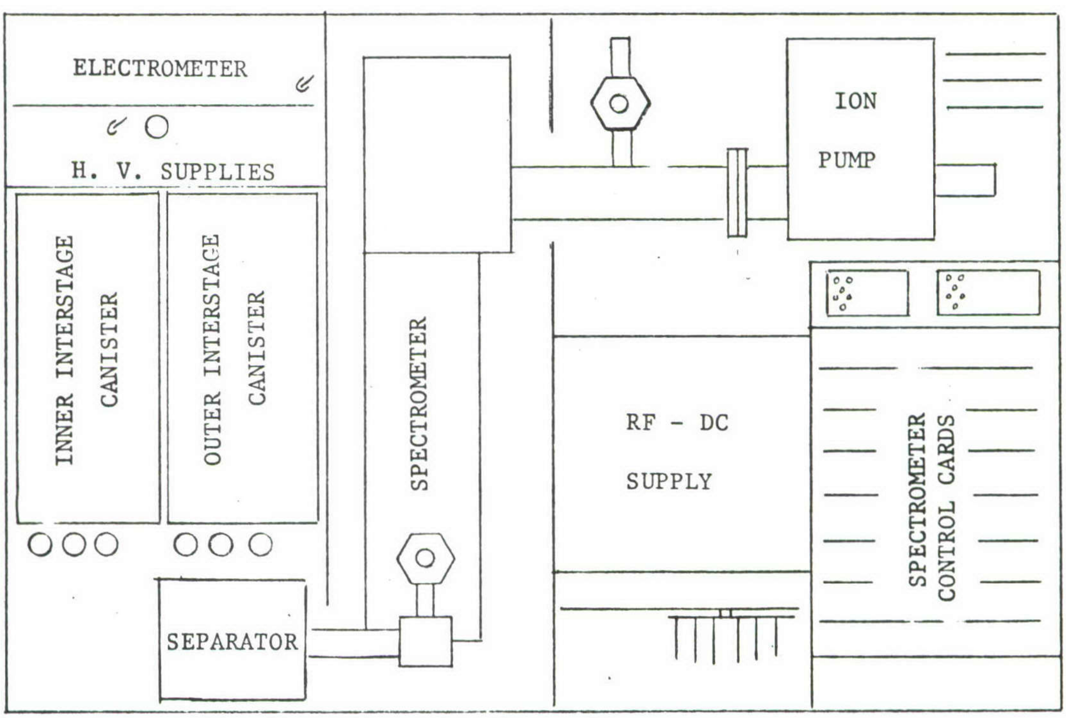


FIGURE 3 Arrangement of Components for the Portable System

alloy and are very strong while being light in weight. The No. 110X case with dimensions 18 x 26 x 9 inches weighs less than 19 lbs. The cases are equipped with piano hinges, and closure is sealed with an elastomeric gasket, which, while not providing a complete hermetic seal, gives reasonable weather protection.

The elements of the system are firmly mounted on frames made up of aluminum alloy channel and angle sections which provide sufficient rigidity for support. The frames are bolted to stress plates rivited to the (bottom) wall of the cases. The spectrometer and its high vacuum housing and pump are fabricated from .050 wall stainless steel (304) tubing. This assembly itself is a structural member along with the frame and comprises most of the weight in case B. Other elements of the system are mounted to the frames with channels and brackets each of which tends to add further to the structural strength of the assembly.

B. SPECTROMETER AND HIGH VACUUM SYSTEM

The quadrupole analyzer is a very precise mechanical assembly. The four molybdenum quadrupole rods ground to precise cylinders are supported on alumina insulators. They must be positioned to a precision of .0001 inch and their position and parallelism must be accurately maintained. Since external forces on the rod structure and its insulators can alter the alignment of the rods by elastic

deformation, the analyzer structure is floated in cylindrical supports at each end of its vacuum housing with a radial clearance of about .001 inch and with axial clearance taken up by a compliant disc. The small radial clearance prevents external forces from distorting the structure but still constrains it when the case is subjected to shock loads.

The housing and support of the quadrupole analyzer forms one element of a four part high vacuum structure. This structure includes, in addition, the ionizer housing, the multiplier housing, and the high vacuum pump. The design was specifically directed to facilitate for access to the ionizer, the quadrupole rods and the multiplier. Each of these elements is provided with its own electrical connections integral to the section of the housing which forms its mounting. The housing itself maintains the necessary juxaposition and alignment of the elements. This is schematically shown in Figure 4. The arrangement adds greatly to convenience and safety for such maintenance procedures as filament and multiplier replacement as may be necessary.

All demountable vacuum joints are clamped with stainless steel bolts and sealed with gold wires whose deformation is captured in both radial and axial clearances (rather than just between two faces), to provide reliable vacuum integrity even when the system

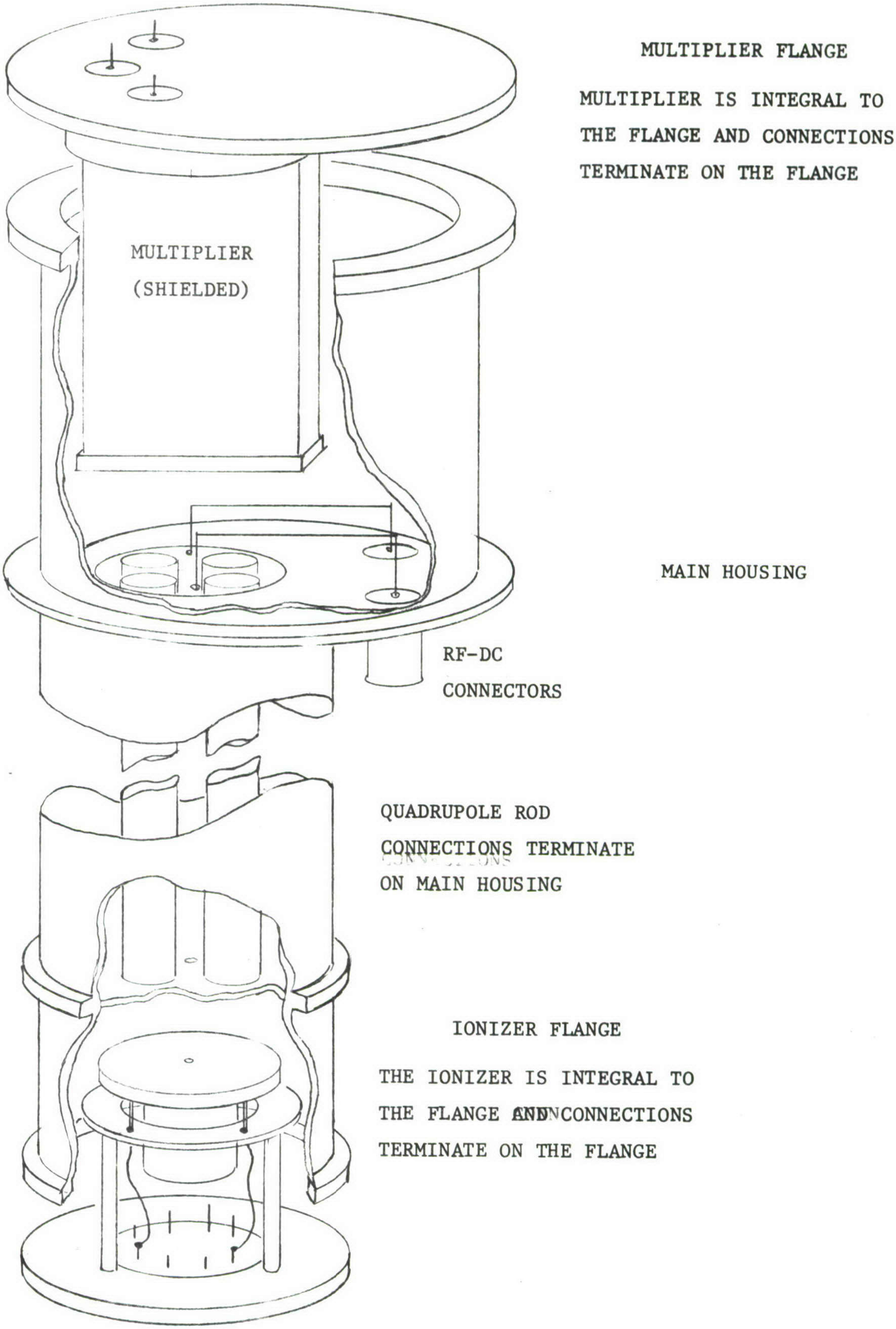


FIGURE 4 High Vacuum Housing of the Mass Spectrometer

is stressed. Other joints in the system are heli-arc welded to provide strength to the relatively light weight structure.

Two ½ inch high vacuum valves are mounted on the high vacuum housing. One of these, adjacent to the high vacuum pump provides for external pumping on the system after opening to atmosphere or prolonged standby. The other may be used to isolate the high vacuum section from the separator. The former valve, which is not in the heated section, has a standard polyimide seal which is rated for temperatures to 300°C (destruction), but which would outgas noticeably at lower temperatures. The latter has been provided with gold seals which may be exposed to bakeout temperatures exceeding 300°C if necessary.

The Perkin Elmer (Ultek) ion pump is rigidly bolted directly to the frame. The rest of the high vacuum housing is supported on a lightweight stainless steel structure which is then bolted to the frame. This support while providing adequate strength is thin enough to reduce thermal losses from the heated spectrometer and to provide some compliance against any displacement of the frame due to twisting or shock loads and differential thermal expansion.

C. SEPARATOR

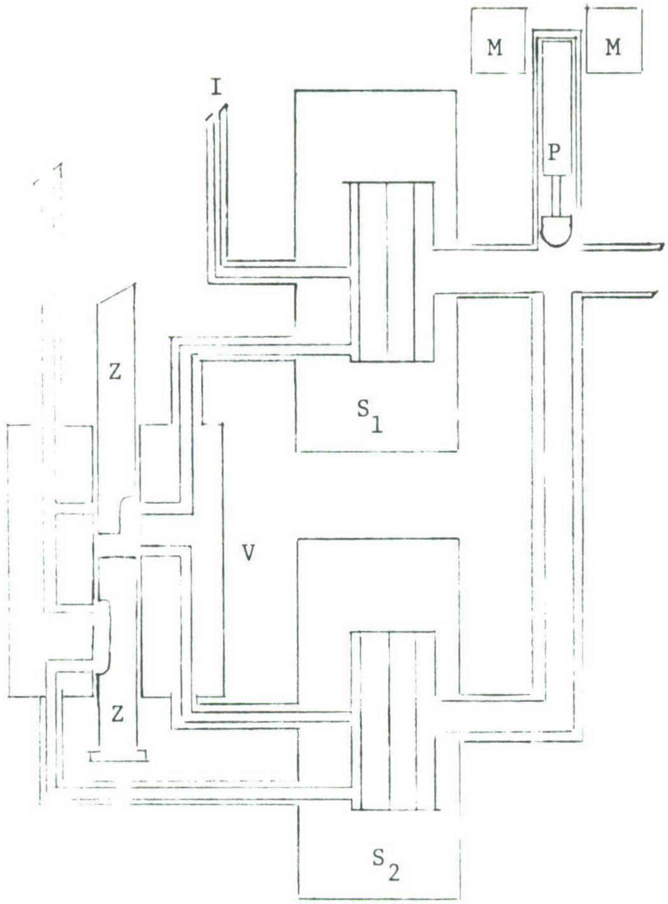
The system is furnished with a dual separator; the two sections of which are operated at different temperatures. In normal vapor sensing operations, the higher temperature section is

set by thermostat to 60° C while the lower one is slightly above ambient. These temperatures are suitable to most materials which are sufficiently volatile that samples do not require heating to furnish partial pressures within the detection range of the system; (nominally greater than 10^{-6} torr). For less volatile materials, usually introduced from liquid samples in the high temperature inlet, the upper separator is used alone, being heated under external control to higher temperatures as required. In this mode of operation, the sample inlet flow bypasses the lower separator, and on the high vacuum line, a magnetically operated valve prevents back streaming of the sample to the lower separator. The details of this arrangement are shown in Figure 5.

The separator itself is constructed after a new design which was undertaken specifically to allow high temperature operation. The two important features of this design are the inclusion of a very fine grid to support the first membrane against atmospheric pressure and the total exclusion of RTV cement in the sample regions. The very fine grid is comprised of a 200 mesh nickel screen .001 inches thick with gold plating for chemical inertness which is mounted on top of a 50 mesh stainless steel screen which provides the principal mechanical support. At

operating temperatures up to 240°C, at which point the softened silicone membrane would otherwise simply be extruded to the point of failure in a very short time by the atmospheric pressure, the very fine mesh provides adequate support for continuous operation. (Test membranes have been operated for two months at this temperature.)

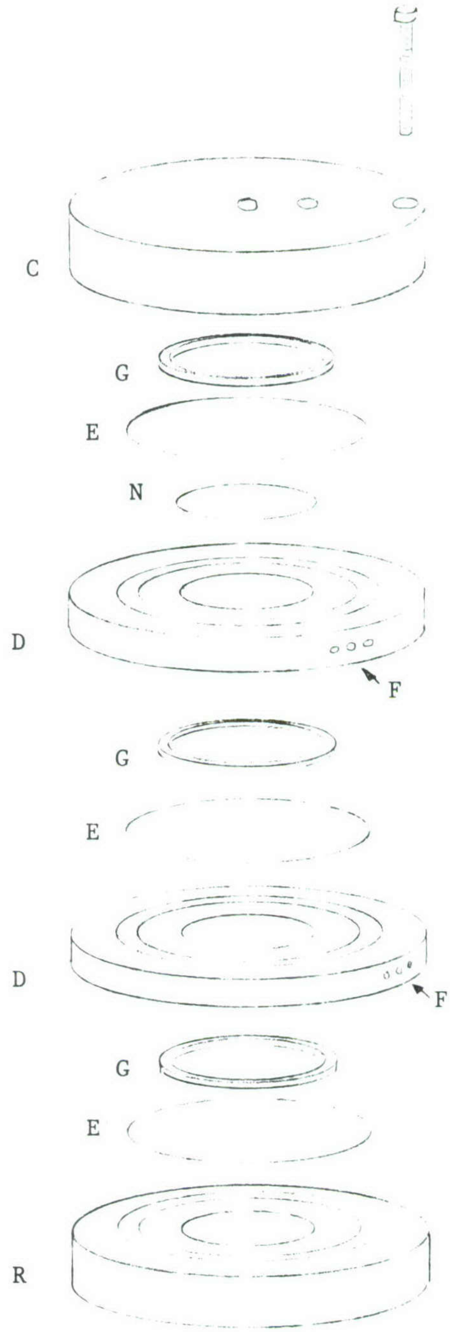
The silicone membranes were formerly mounted in the separator with silicone cement. Although the cement is nominally identical to the membrane material, at higher temperatures, the spectrum showed very large peaks of silicone fragments indicating less complete polymerization in the cured cement. At temperatures above 180°C these peaks were so large as to obscure the detection of low levels of sample. In view of this, a method was devised to capture the membrane and to form the vacuum seals in the separator using polished surfaces and polyimide sealing rings. Details of this sealing method are shown in Figure 5. Sealing forces required are very low due to the very small area of contact at the tapered upper profile of the elastomeric polyimide ring; thus, the separator can be assembled with small (#2-56) screws using very light torque. The assembled separator is held in a close fitting aluminum ring which provides uniform heat distribution and mechanical support against lateral displacement of the seals which would endanger



A. SEPARATOR, SAMPLE DISTRIBUTION SCHEME IN SECTIONAL VIEW

LEGEND FOR A. AND B.

S_1: Separator hot section.
S_2: Separator cold section.
V: Valve body.
Z: Spool.
I: Inlet.
H: Exhaust to sample pump.
M: Magnet.
P: Poppet.
C: Cover.
G: Gasket.
E: Membrane.
N: Fine mesh.
D: Membrane support discs.
R: Receiver.
F: Interstage pumping port.



B. EXPLODED VIEW OF SEPARATOR

FIGURE 5.
Separator Structure

the seals. The two aluminum rings are firmly supported by a thin stainless steel bracket which anchors the structure to the frame and, at the same time, serves to isolate the parts thermally. Interstage valves and pumping lines are provided to accomplish the necessary interstage pumping. To preclude stress on the separator and valves, short sections of flexible teflon tubing are included in the interstage pumping lines. The interstage pumping requirements are met by two zeolite canisters which are fitted with the necessary valves and quick disconnect fittings for daily pumpdown needs and for isolation as required. All valves used were either specially fabricated or modified from commercial units. Pump-down and isolation valves have been provided with polymide elastomeric stem tips for sure sealing.

D. ELECTRONIC ELEMENTS

The remainder of the mechanical assembly is principally comprised of the mounting of the many electronic elements of the system. Since these parts are light in weight, they do not pose difficult mounting problems. Careful attention is given to electrical shielding and isolation where necessary. The entire analog system is electrically isolated and grounded to the frame at a single point in order to minimize ground-loop and noise problems. The RF-DC supply to the quadrupole is housed in a heavy gold plated brass case

for mechanical rigidity required to maintain tuning adjustment. Other electronic elements are less critical mechanically and are mounted on conventional circuit cards retained in various card cages mounted in both cases. Card plugs and elastomeric card guides support each card on three sides. Heavy components are secured to the cards with RTV cement.

Cooling for electrical components is accomplished by convection, conduction and forced air cooling. Smaller heat loads are primarily cooled by convection on the boards or various panels. The principal heat generated in the RF-DC supply, occurring in the power transistor, is dissipated convectively with an oversized heat sink and ample ventilation. Other elements in case B which dissipate power, including the ion pump and electron multiplier power supplies and the filament transformer and rectifier, are cooled by conduction to the main frame and the internal covers. In case A, the greatest heat dissipation occurs in the main power regulator. This heat load which can reach 100 watts under high line voltage conditions is removed by forced air across the heat sinks and four high power dissipation resistors. Air to the fan is drawn from the interior of the case and thus the cooling arrangement serves also to cool the remainder of case A.

IV ELECTRICAL AND ELECTRONIC HARDWARE

The vapor detection system requires complex electrical and electronic components and interconnection. This hardware will be described below. Reference will be made to section VII (MAINTENANCE) which includes detailed circuit diagrams. The electrical and electronic equipment is divided into several categories described below.

A. POWER SYSTEM

Primary power for system operation is drawn from commercial lines at 110 volts, 60 Hz. Total power consumption is approximately 300 watts. When primary power is turned on, the entire operation including high vacuum pumping is furnished from the lines. When primary power is disconnected, the ion pump may be operated from a low power D. C. source of 12-28 volts. A standby power supply for this purpose, operating itself from commercial 110 volts, 60 Hz lines, is furnished. In addition, portable or vehicular battery supplies may be used. Switching between external and system primary power is automatic and requires no operator attention. Standby power may be introduced through an electrical receptacle from the outside of the closed case, (case B). Portable batteries may be installed inside case B and connected through a plug inside the case for

shipment where no standby power can be made available. Two standard heavy duty Leclanche lantern batteries of 4 type F cells each, furnishing 12 volts when connected in series have been used to furnish standby power for more than 24 hours. Alkaline batteries of equivalent size should increase the standby time by a considerable margin.

The vapor detection system requires a large number of isolated regulated direct current power supplies. For purposes of economy and moderate weight, the most appropriate choice for the main power system is a transformer isolated series of alternating current sources operated at frequencies above the audio range, each furnished with its own rectifier, filter and regulator. In the system furnished, commercial power at 60 Hz is converted to direct current at about 150 VDC. This DC supply is regulated to 117 volts and applied to two DC-AC converters having output transformers furnished with the multiple secondary windings required for the various isolated supplies. This converter, operating at 40 KHz requires very little weight in iron. The two converters together weigh 40 ounces, while a 60 Hz transformer of the same power capability would weigh at least 25 pounds. These converters were supplied by the Arnold Magnetics Corporation of Culver City, CA.

The main power system with its rectifiers, filters and regulators furnishes a total of 14 DC power supplies to the vapor detection system. Circuit details of the supply section may be found on sheets SN 17 and SN 26. The 60 Hz AC-DC converter with its regulator and current protection provision is shown on SN 26. A simplified schematic of this section is shown in Figure 6. The output of the main pass transistor is maintained at 117 volts through its drive from the emitter follower Q_2 which is referenced to the zener diode. If excessive current is sensed (in the .25 ohm resistor), the amplifier, A, switches Q_1, disabling the drive to Q_2 and shutting down power. Since the amplifier is biased from the output, the shutdown latches off, and a reset signal must be supplied to start or restart the supply.

The 117 VDC is connected to the two DC-AC converters as shown on sheet SN 17. Secondary windings are connected to conventional power supply arrangements. A typical regulated supply is shown on sheet SN 21. In this particular supply, as in several others, protection against unexpected overvoltage is provided through its use of zener diodes which will act as shunt limiters until the replacable fuse opens the circuit. This provision protects the very large number of integrated circuits from destruction by high voltage transients.

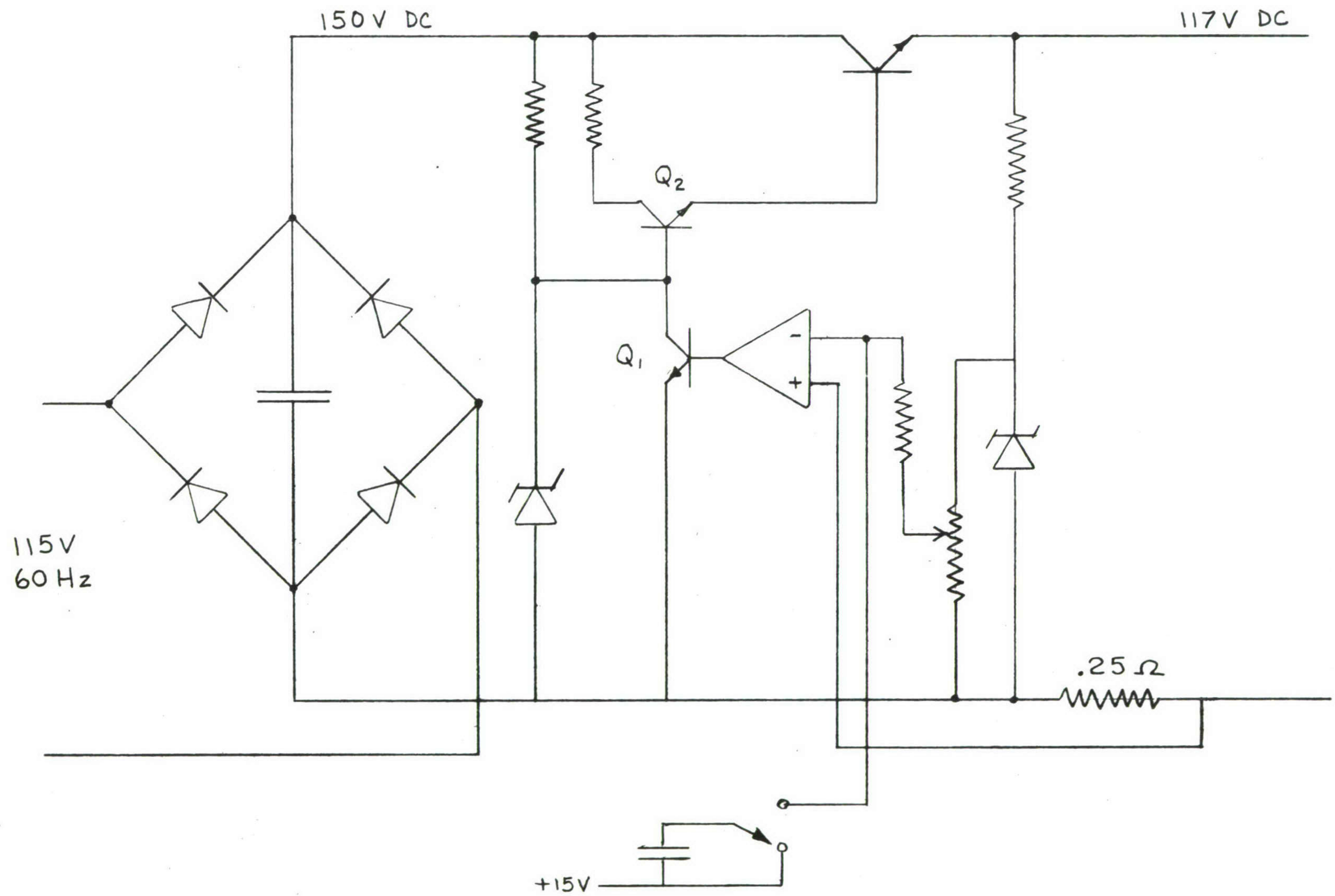


FIGURE 6.
117 V DC Regulator
& Current Limiter

40 KHz current to the filament transformer is controlled by the pass transistor, Q_4, and is regulated by an error signal developed in the servo amplifier, A, which senses the emission current flowing through R_{12}. Sheet SN 24 also shows a current limiting provision which protects the filament from excessive current when no emission current is sensed. The filament requires power of about 20 watts at low voltage and high current, and the method of regulation on the primary side of the filament transformer at high voltage and low current permits higher efficiencies in power utilization.

The ionizer diode is usually operated at 70 volts, and electrons of this energy transit the interior of the anode region several times before being captured on one of its grid wires. When a collision of an electron with a molecule occurs within the anode structure, ions are formed, and positive ions are extracted from this region by a small extraction potential applied to the focus electrode located between the quadrupole analyzer and the ionizer. The ionizer diode and focus electrode voltages and the offset voltage which determines ion energy in the quadrupole are furnished by adjustable supplies shown on sheet SN 23.

B. SPECTROMETER ANALOG SYSTEMS

1. General: The quadrupole spectrometer is basically an analog device. Ions are formed in the ionizer section which is furnished with various constant DC potentials. These ions pass into an analyzer section, (the quadrupole). Constant DC and stable RF voltages applied to the quadrupole rods mediate the transmission of the ions to the detector section so that only ions of a single mass are transmitted at any one time. These ions arriving at the detector from an analog current which, when amplified, first in an electron multiplier and then in a multirange electrometer, constitutes the mass peak signal.

2. Ionizer: The ionizer is of the familiar electron impact design as furnished by the spectrometer vendor. It is patterned after the Alpert ionization vacuum gauge, using a tungsten 3% rhenium filament operated outside an anode structure formed by a cylindrical grid. These two electrodes form a diode which is operated in temperature limited emission with a current of about one milliampere. Filament heating is controlled with an electrical servo to maintain constant diode current. A simplified schematic of this control is shown in Figure 7. The detailed circuit may be found on sheet SN 24. As shown in Figure 7, the primary

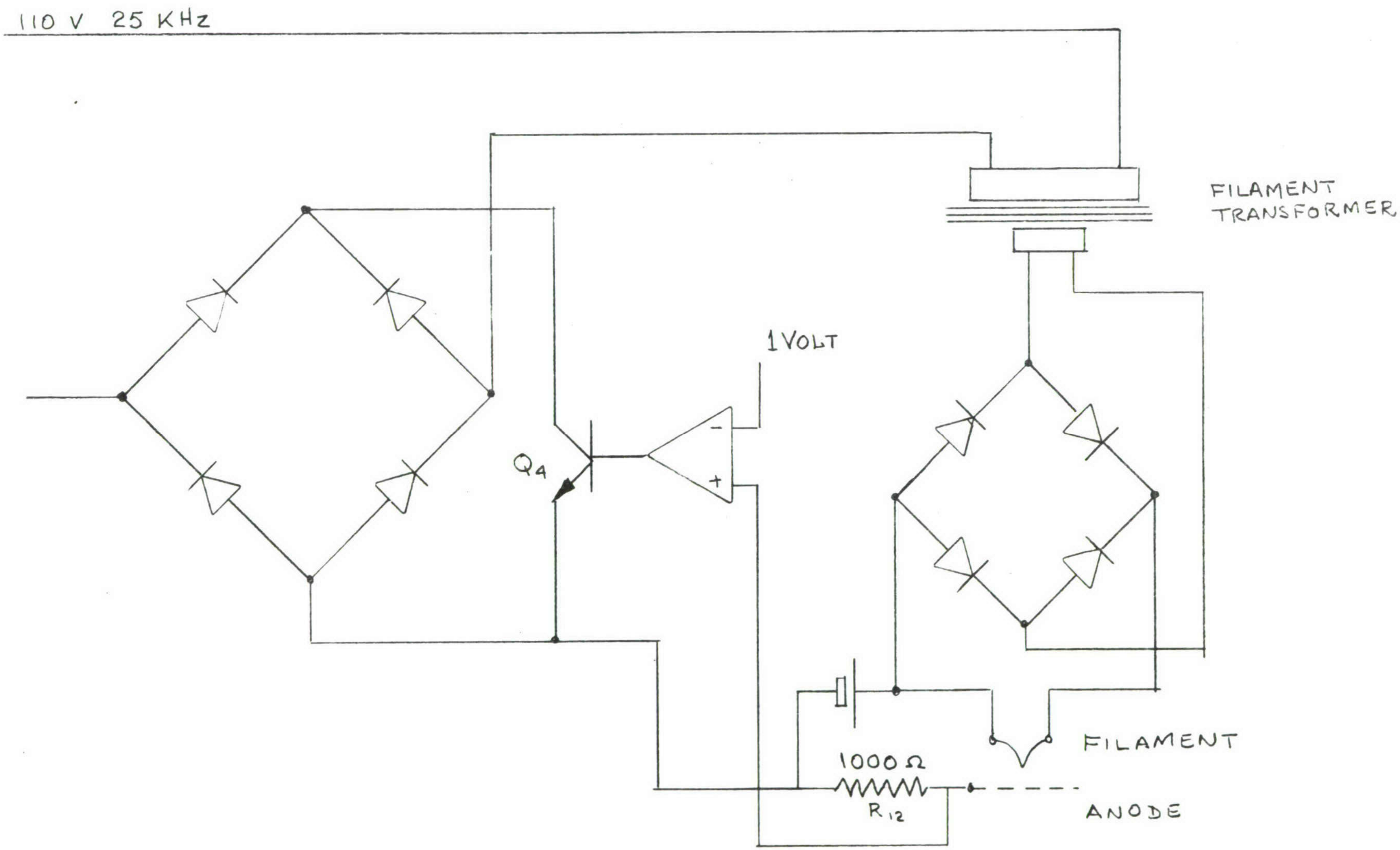


FIGURE 7
Filament Current Regulator

3. <u>RF-DC Supply</u>: The quadrupole filter requies RF and DC voltages to about 4000V pp and ± 700V respectively. Fluctuation in these voltages must be held to less than 0.1% at the higher values in order to maintain high resolution and transmission. In the supply of these voltages used in the portable vapor detection system, the constant RF-DC voltage ratio, required to about 0.01%, is maintained simply by deriving the DC through a rectifier and filter directly from the RF voltage applied to the quadrupole rods. The regulation of the RF voltage itself is maintained by an electrical servo, which compares a fraction of the RF voltage with an analog control voltage and generates a correction signal to the RF supply when these do not track.

The details of the RF-DC system are shown on sheets SN 4 and SN 5. A simplified schematic appears as Figure 8. When RF currents flow in the transformer, the rectifiers V_1A and V_1B will develop proportionate DC potentials on C_7 and C_8, providing the necessary DC drive to the rods along with the RF from the transformer. Resistors R_4, R_5, R_6, R_7 are chosen to refine the RF-DC ration and to allow rapid changes in the RF and DC levels. Trimming of the RF-DC ratio and balance is accomplished through R_8-R_{11}. A portion of the RF voltage appears at points A and B. This portion is rectified by V_2 and is delivered as

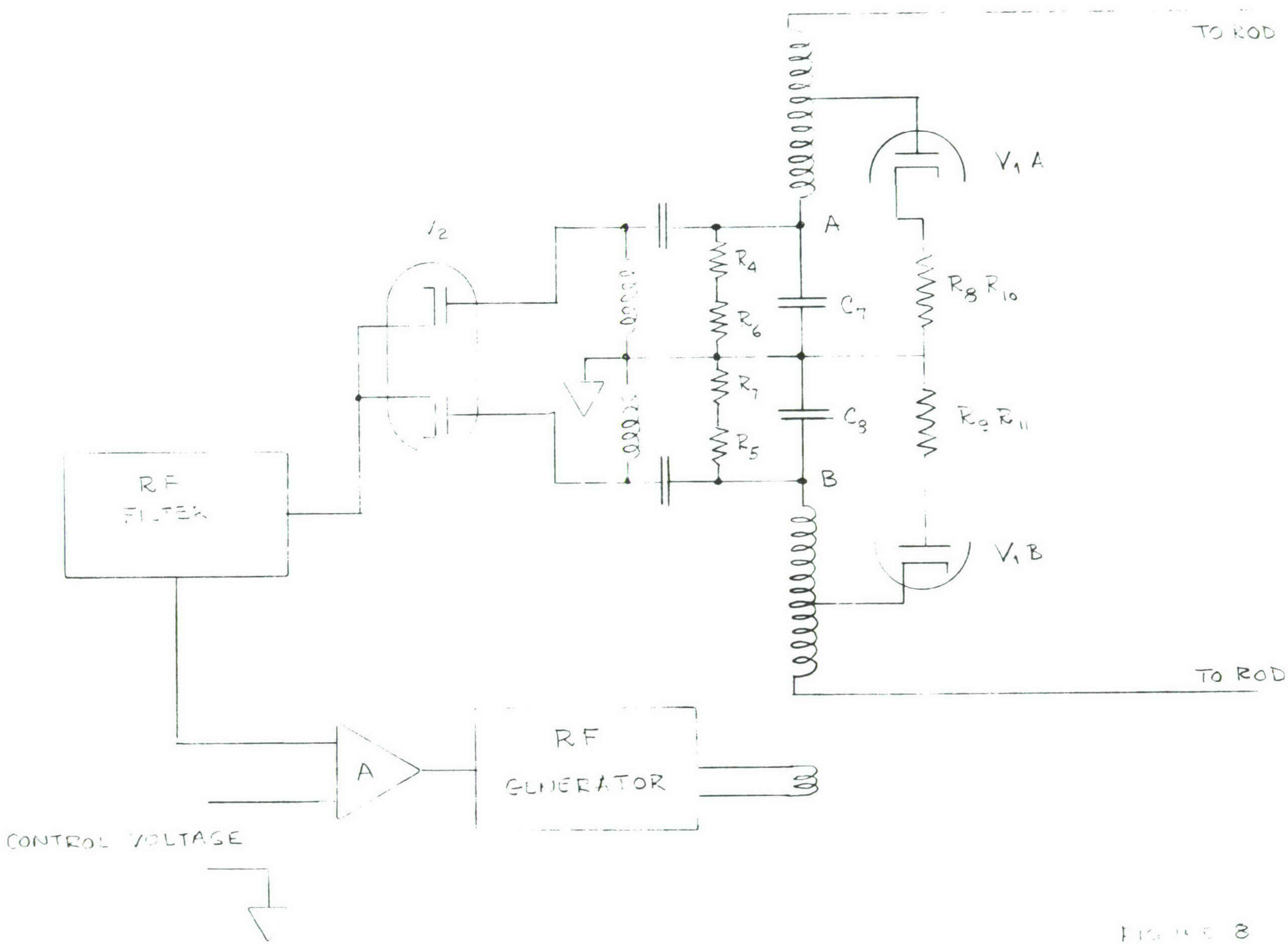


FIGURE 8
RF - DC Driver. Level
Detector and DC Source

a comparison signal to the amplifier A whose output signal determines the drive level in the RF generator. Since the comparison is to the control voltage, the outputs to the quadrupole rods will track the control voltage applied.

4. Electron Multiplier and Electrometer: The ions transmitted through the quadrupole analyzer are accelerated and strike the first dynode of an electron multiplier operated at about -2000 volts. The ions dislodge electrons which cascade through the multiplier structure with a gain in electron current of $10^4 - 10^5$. The current collected at the output of the multiplier is delivered to a multirange electrometer. Electron currents of 10^{-12} ampere give an output of 0.1 volt on the most sensitive scale while currents of 2×10^{-8} give an output of about 5 volts on the least sensitive scales. (These four scales arranged with sensitivities which descend by powers of $8 = 2^3$.)

The multiple scale electrometer has been very satisfactory to the accommodation of a wide dynamic range of input currents. It is unconventional in design, and a patent disclosure was submitted covering its novel features. The complete electrometer including a solid state switched current integrating feature is shown in sheets SN 7 and SN 8.

A simplified schematic diagram of the operating principle is shown in Figure 9.

In this figure, clearly, the output of A_1 will be at 10^{-11} amperes per volt referred to the input current, provided that no current passes the diodes leading to later stages. The output of A_2 will be one tenth this, or 10^{-10} amperes per volt even when the diodes $D_5 \ldots D_8$ do not conduct, so long as R_6 and R_7 are in the ratio of 9:1. Similarly, the outputs of A_3 and A_4 will scale at 10^{-9} amperes per volt and 10^{-8} amperes per volt respectively. As A_1 nears saturation, at about 10^{-10} amperes, diodes $D_5 \ldots D_8$ begin to conduct, relieving A_1 of further current, and extending the output of A_2 beyond the level determined by the input coming from R_6 R_7. Similarly, when A_2 nears saturation, the input current is transferred to A_2 and so on. Not shown in Figure 9, but appearing in sheet SN 7 are four sense amplifiers, one from each range. These sense amplifiers indicate to the user which range should be used to read input current. Figure 10 shows the output characteristics for a four decade electrometer. The points marked T_{1-2}, T_{2-3}, T_{3-4}, indicate the point at which input current is transferred to each of the amplifiers, A_2 A_3 A_4.

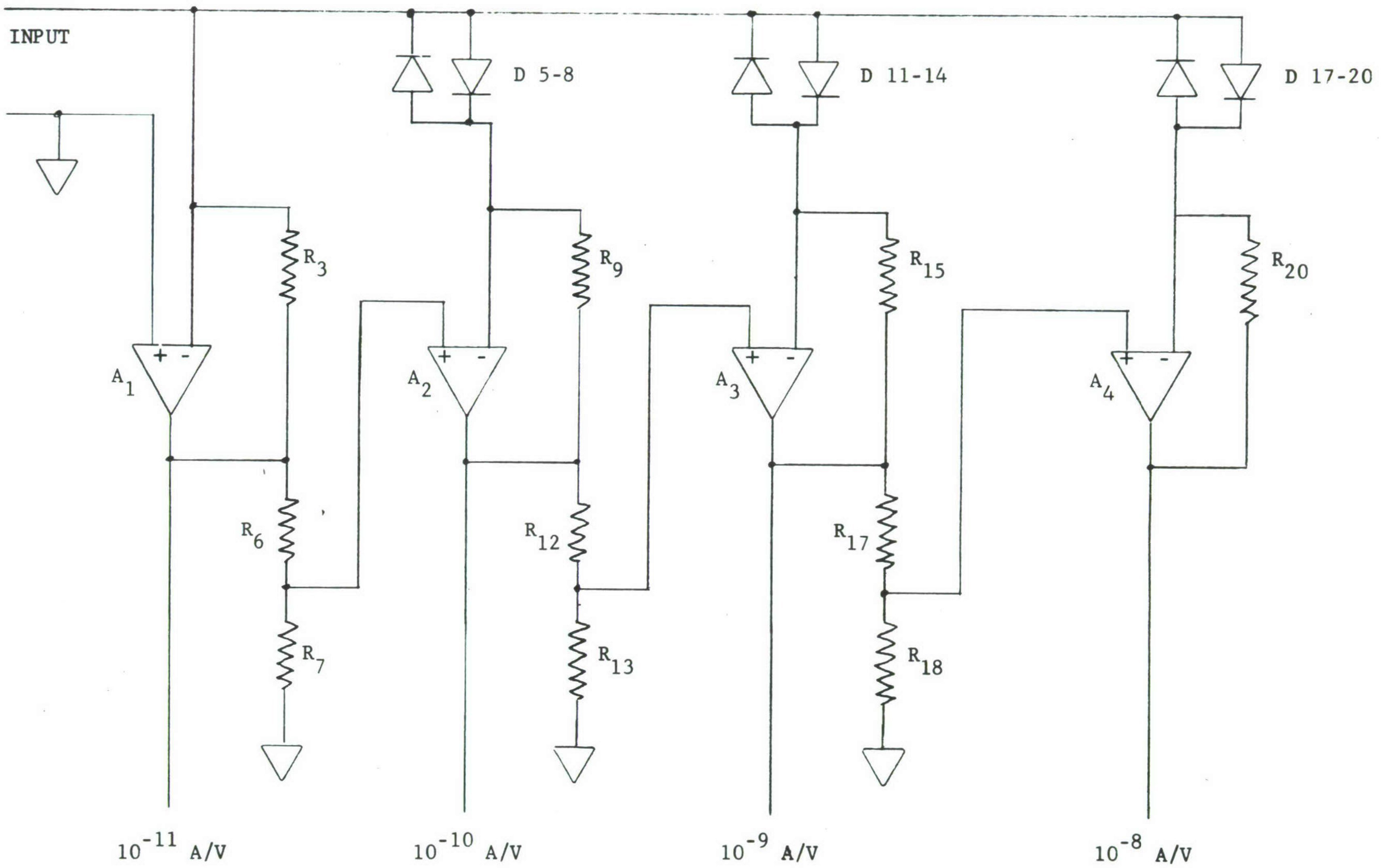


FIGURE 9.

Autoranging Electrometer Scheme

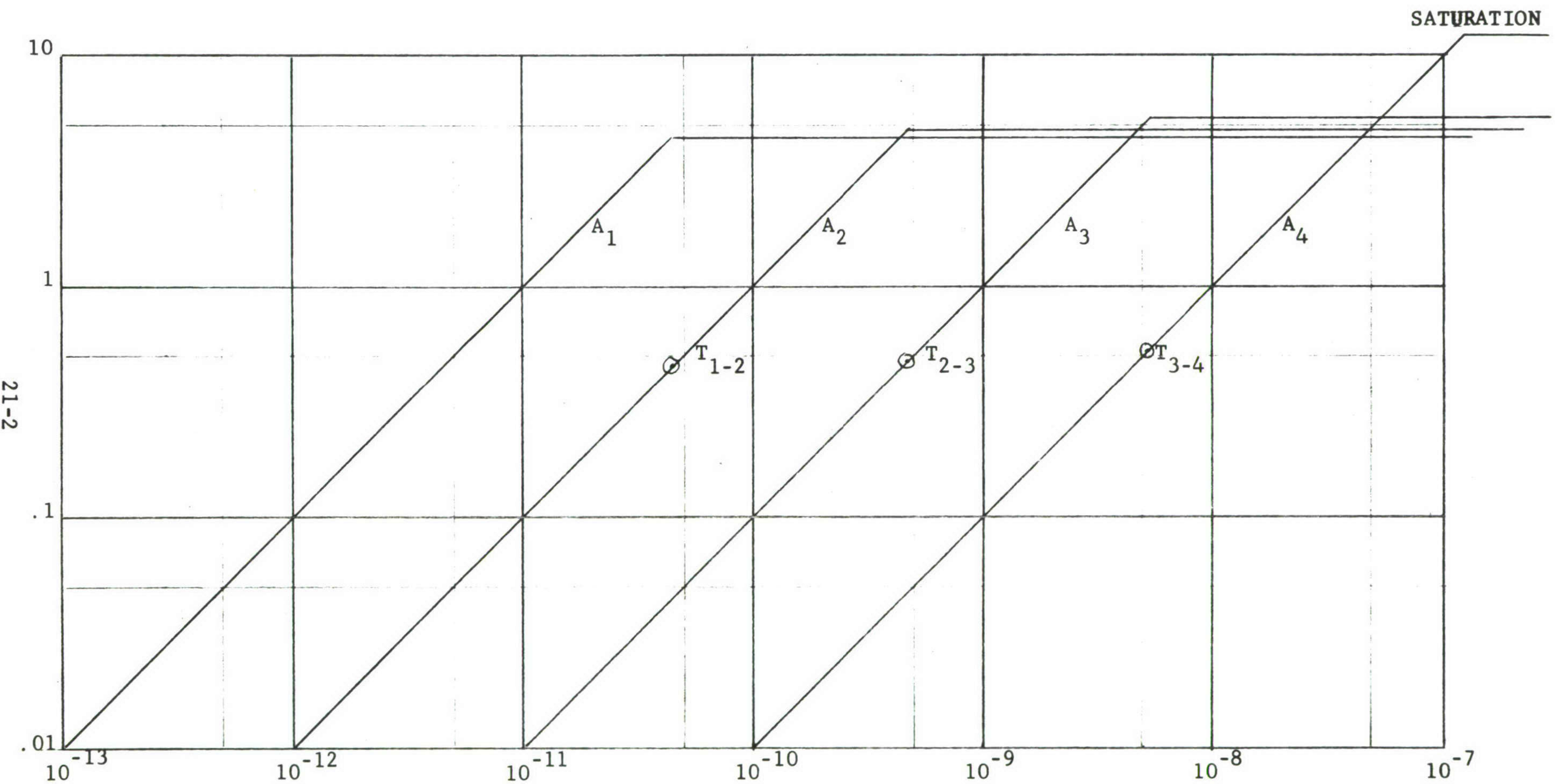


FIGURE 10.

Response of the Auto-
ranging Electrometer

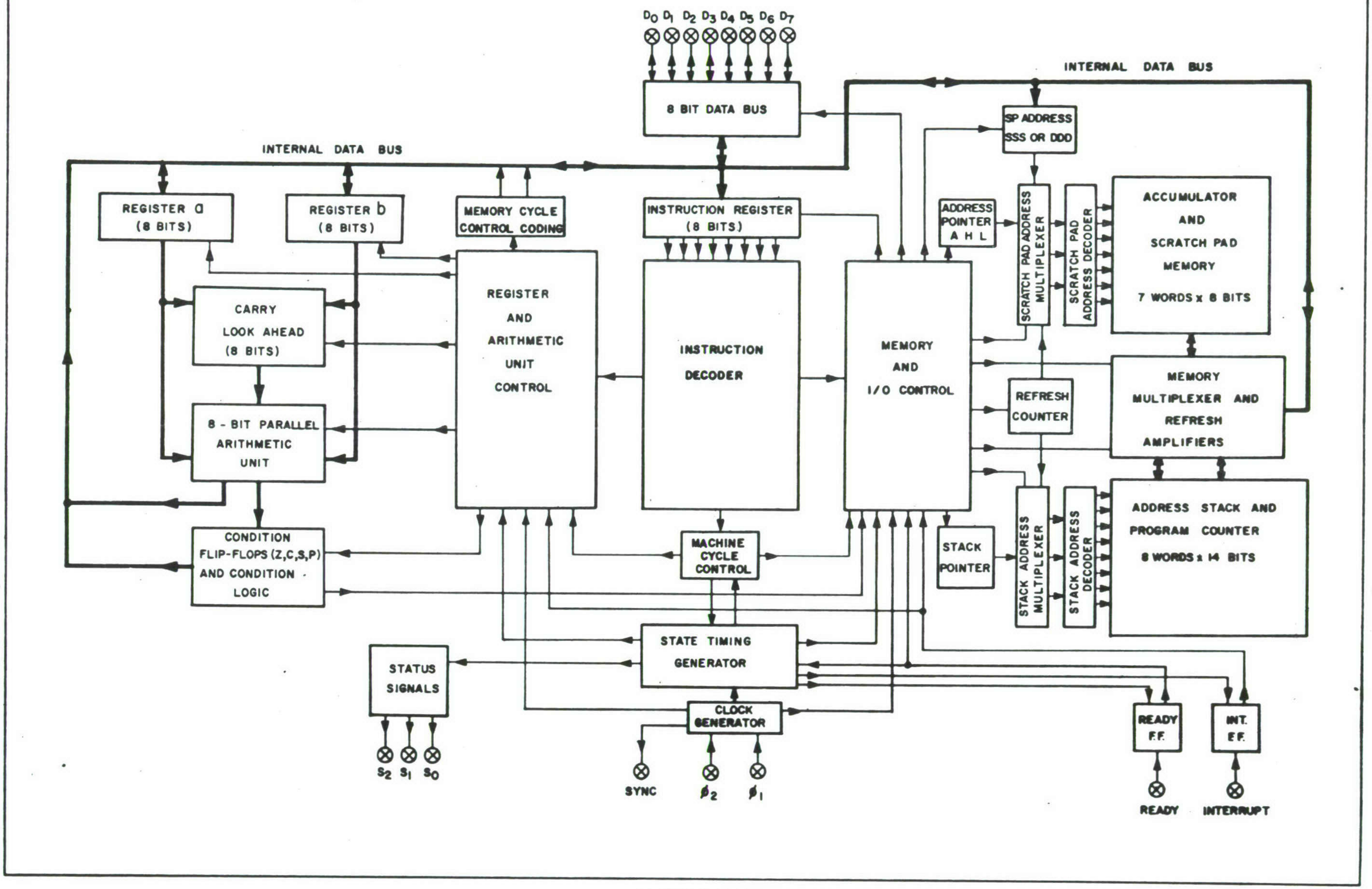
Also appearing on sheet SN 7, are the switching provisions for the integrating mode of the electrometer. The switching function is controlled by digital commands through U_1. Actual discharge of the integrating capacitors is accomplished by servo amplifiers U_{10}, U_{11}, U_{12}, U_{13} which supply currents to the inputs of A_1 A_2 A_3 and A_4 until the outputs settle to zero. The servo amplifiers are disconnected during integration through the action of the FET switches and isolating diodes.

C. DIGITAL SYSTEM

The operation and control of the vapor detection system is entirely under digital control. Control routines are maintained in the stored program of a microcomputer. Access and selection of routines is available to an operator through front panel switches. The digital operation is interfaced to the analog requirements through appropriate digital to analog and analog to digital converters. The digital system is organized around three data busses as shown in sheet SN 35. The A-buss carries 16 bits, 14 of which constitute the address line and 2 of which are control indicator lines. The A-buss is actuated by the computer and is sensed and decoded by the other elements attached. The I (input) buss carries 8 bits of data to be read into the computer as required. The 0 (output) buss carries the data output from

the computer. These data are addressed by the A-buss to selected terminal elements. In addition to the data busses, various control lines are routed between elements of the system. The computer and other elements are separately described below.

1. General Purpose Digital Computer: The computer used in the portable vapor detection system was specially designed and developed for this application in order to accommodate size, weight, and power constraints. The computer itself is comprised of two 4 by 6 inch circuit cards; the memory and accessory elements are distributed on an additional 8 cards in the left hand card cage of case A. The computer was designed around the Intel 8008 microprocessor. The processor itself is an 18 pin microelectronic device using MOS technology. It is a parallel access 8 bit byte oriented processor with an externally initiated and clocked variable cycle time of from 7-12.5 microseconds. The device is provided with an 8 level program counter of 14 bits per level for nesting of sub-routines, a 7 level by 8 bit set of working registers, an instruction register and ALU control section, the 8 bit ALU itself and the necessary additional decoders and control elements for moving and processing data in accordance with the versatile instruction set. A block diagram of the device is shown in Figure 11.



8008 Block Diagram

FIGURE 11.

The 8008 communicates with the external world through 8 bit words transmitted in both directions via an 8 bit internal data bus. Internal cycling of the device is initiated externally and controlled internally cycle status is communicated externally through status lines and a synchronizing signal. A high logic level on the ready line or the interrupt line will initiate an operating cycle. Figure 12 shows the operating cycle of the 8008. Entry is either from "WAIT" with a "READY" signal, or from the interrupted condition leading to T 11. (An interrupt initiates the escape from a stopped condition.)

During T1 or T11 and T2 two bytes of address and control information are presented to the data lines. This information is captured in two 8 bit latches external to the 8008, (U_{16}, U_{17}, U_{18}, U_{19} on SN 28). This address and control information is held and is available during the WAIT and subsequent cycles. Normally it is decoded to actuate an input device such as memory and thereby have data ready for the 8008 data lines during the appropriate part of T3. The decision and exact time of data input is mediated by the control bits held on U19 and clock and synch information. (Trace U19 {15, 16} , U3 { 12, 13} ; U12 {1, 2, 13} , U4 { 3 } , U3 { 9, 10} ; U17, U18 on sheet SN 28.) The 8008 accepts this information and takes

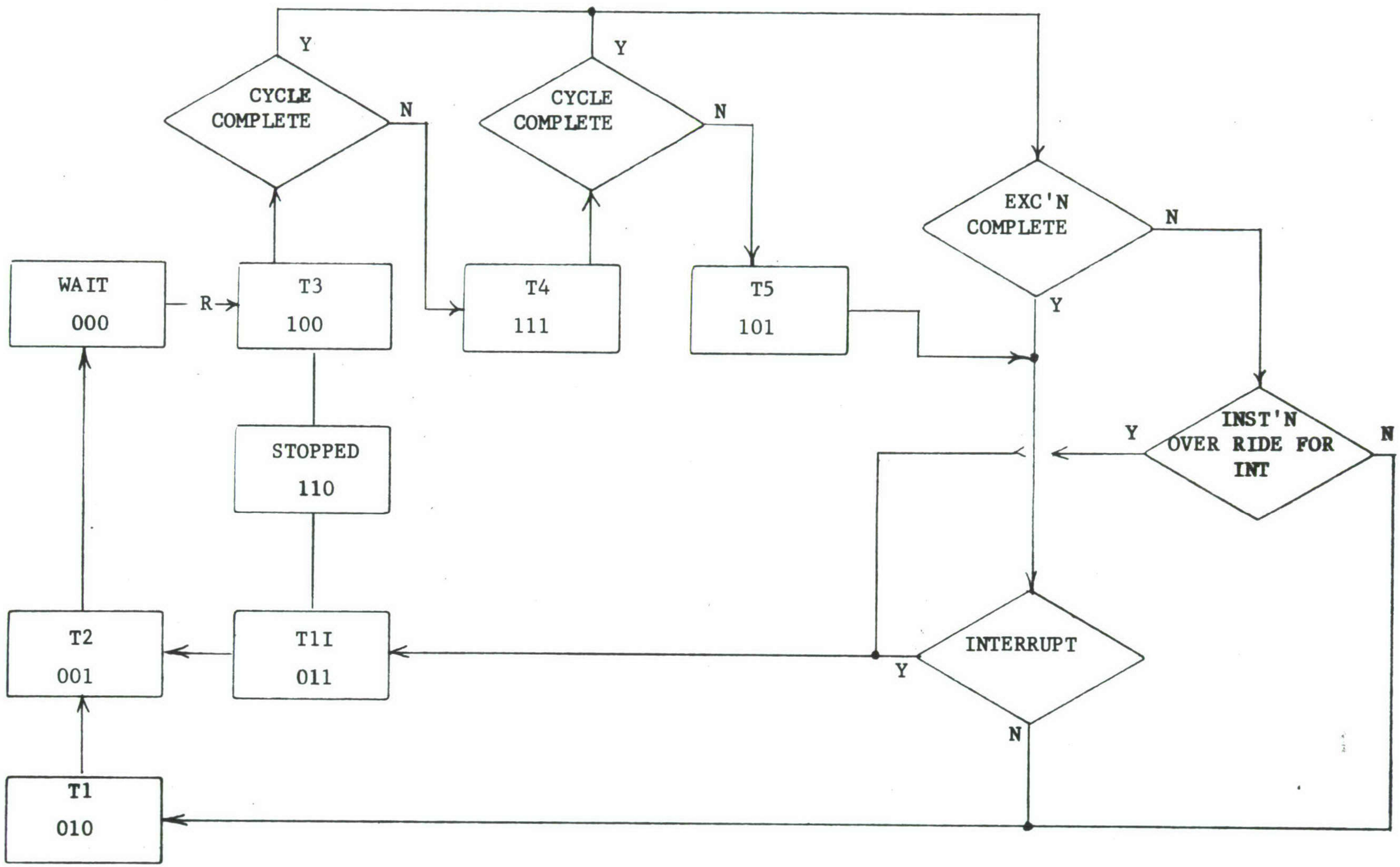


FIGURE 12.

Intel 8008 Internal Flow Diagram

appropriate action during subsequent steps in the cycle. For example, if the input data at T3 is a move word instruction to transfer data from the B register to the C register in the 8008, (11010001), then in T4, data from the B register are transferred to a working register, b, and in T5 data from this working register are transferred to the c register. At the completion of these two steps for this instruction, the operation cycle advances automatically to T1 and T2 at which times new address and control bits are cycled through the data lines for external capture.

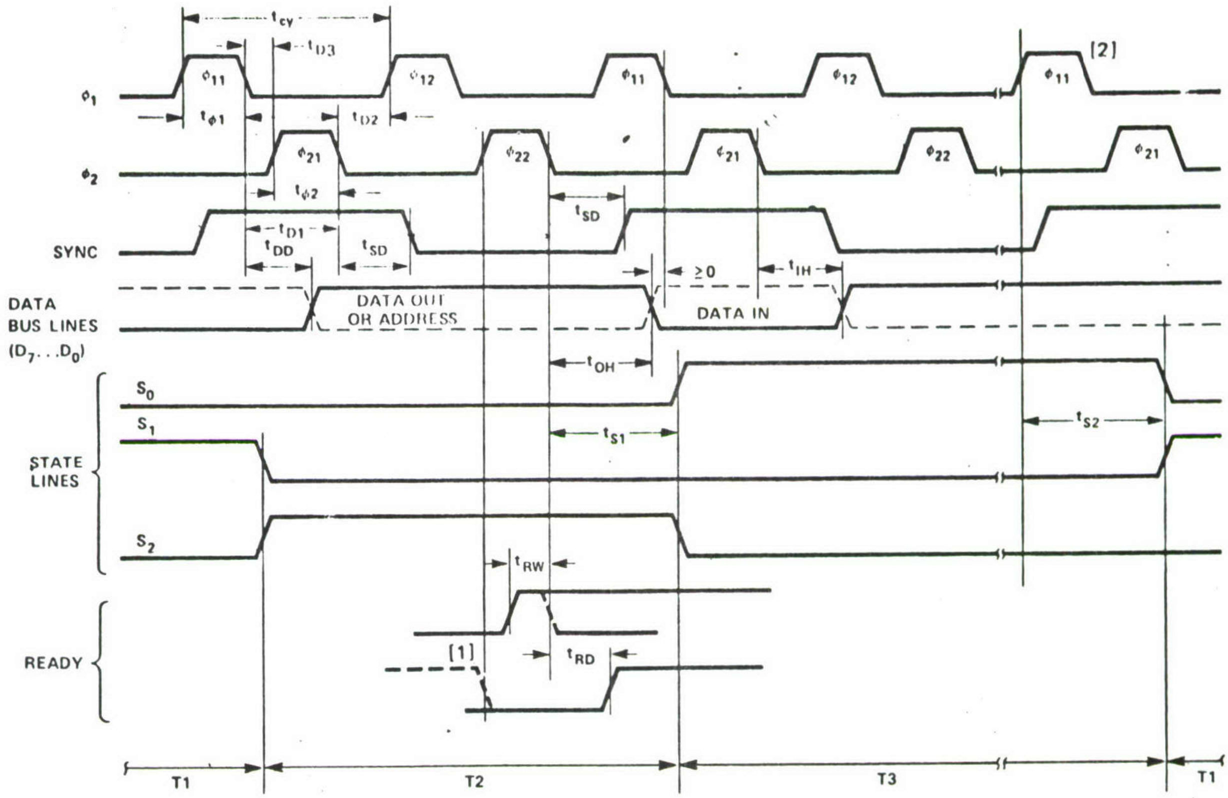
If the instruction or other input data are faulty or mistimed, the computer may enter the STOP condition immediately. An instruction of 00000000 or one of 11111111 on the I-buss will lead to a halt. Instructions in error may also simply result in mis-execution of the program with no halt at the time of error. Proper timing of the input data and presentation of proper data from memory and other sources preclude such undesired miscues.

In addition to several important decoding procedures which supervise the routing of data to and from the computer, there are several other sequences generated whose timing is critical to the operation of the computer. Not all of these will be described; however, by way of example, the timing for an interrupt cycle is described as follows. The 8008 can accept an interrupt command

at any time except within 200 nanoseconds of the falling edge of the phase 1 clock pulse. In order to ensure the safe entry of an interrupt, the external command to interrupt, (which may arrive at any time), is held up in a flip flop circuit, U11 {9-13} and is transferred to the interrupt line via U4 precisely at the rising edge of the phase 1 clock which places this signal more than 200 nano seconds from the falling edge. (The phase 1 clock pluse has a width of at least 700 nano seconds.) The timing requirements for data routing are summarized in Figure 13 which shows a typical step of the operation cycle, here labeled T3. Timing fiducials are taken from the clock (input) and SYNCH (output) pulses. The time margins specified by the manufacturer are shown in the accompanying table.

2. Memory: The computer operates with a memory system which includes 1792 8 bit words of read only memory, (ROM), and 1024 8 bit words of random access memory, (RAM). The ROM holds the stored program while the RAM is used for data and program variables. The ROM is made up of seven MOS devices each containing 256 words of 8 bits. The memory is static and each device decodes 8 bits of address. An additional 7 bits of address is decoded externally to select ROM in blocks of 256 words, (up to 14 blocks are directly accessible).

TIMING DIAGRAM



[1] READY line must be at "0" prior to ϕ_{22} of T_2 to guarantee entry into the WAIT state.
[2] INTERRUPT line must not change levels within 200ns (max.) of the falling edge of ϕ_1.

SYMBOL	PARAMETER	8008 LIMITS		8008-1 LIMITS		UNIT	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
t_{CY}	CLOCK PERIOD	2	3	1.25	3	μs	t_R, t_F = 50ns
t_R, t_F	CLOCK RISE AND FALL TIMES		50		50	ns	
$t_{\phi1}$	PULSE WIDTH OF ϕ_1	.70		.35		μs	
$t_{\phi2}$	PULSE WIDTH OF ϕ_2	.55		.35		μs	
t_{D1}	CLOCK DELAY FROM FALLING EDGE OF ϕ_1 TO FALLING EDGE OF ϕ_2	.90	1.1		1.1	μs	
t_{D2}	CLOCK DELAY FROM ϕ_2 TO ϕ_1	.40		.35		μs	
t_{D3}	CLOCK DELAY FROM ϕ_1 TO ϕ_2	.20		.20		μs	
t_{DD}	DATA OUT DELAY		1.0		1.0	μs	C_L = 100pF
t_{OH}	HOLD TIME FOR DATA OUT	.10		.10		μs	
t_{IH}	HOLD TIME FOR DATA IN	[1]		[1]		μs	
t_{SD}	SYNC OUT DELAY		.70		.70	μs	C_L = 100pF
t_{S1}	STATE OUT DELAY (ALL STATES EXCEPT T1 AND T1I) [2]		1.1		1.1	μs	C_L = 100pF
t_{S2}	STATE OUT DELAY (STATES T1 AND T1I)		1.0		1.0	μs	C_L = 100pF
t_{RW}	PULSE WIDTH OF READY DURING ϕ_{22} TO ENTER T3 STATE	.35		.35		μs	
t_{RD}	READY DELAY TO ENTER WAIT STATE	.20		.20		μs	

[1] t_{IH} MIN ≥ t_{SD} [2] If the INTERRUPT is not used, all states have the same output delay, t_{S1}.

FIGURE 13.

The first ROM card is shown in sheet SN 30. The high bits for decoding are processed in U7, U8, U9. Bit A_{14} distinguishes a read cycle and Bits A_{13} and A_{12} distinguish ROM from RAM. Bits A_{11}, A_{10}, A_9, A_8 select ROM blocks. The decoding of A_{14}, A_{13}, A_{12}, A_{11} is extended to the second ROM board whose circuit is identical to sheet SN 30 except for the omission of U8 and U9. Expansion of ROM to a total of 7680 words is possible with the address scheme devised.

When a ROM address with read control is placed by the computer on the A-buss, the ROM responds by placing the appropriate word on the I-buss. The computer at this point is cocked to enter a WAIT step, pending issuance of a signal on the ready line. The cycle time of the ROM is sufficiently fast, (maximum of 1 micro-second), that no wait is necessary; therefore, the decoded address automatically sets the ready line and the computer will skip the WAIT step and proceed directly to T3, thereby speeding up the computer operation.

It will be noted that in the decoding on the first ROM board, blocks zero and two are reserved for other functions. These blocks are designated specifically as follows: Block zero accesses a start routine, the operator control switch positions, the spectrometer, and the hardware multiply and divide functions.

Block two accesses the display. The extensive input-output requirements represented in these functions exceed the normal input-output capability of the 8008. The fact that its cycling is under external control at all times allows the use of the entire memory field for input-output functions. This method of access has a great advantage for application to systems requiring extensive communication with external devices.

The 1024 bit RAM is made up of 8 MOS static devices each comprising a 1024 word by 1 bit memory. Ten address bits are decoded on the devices. The remaining 6 bits are decoded as shown in sheet SN 31 through U10, U11, U12, U13. The RAM circuit board has decoding facility to manage a second block of 1024 words of RAM and further expansion to add three more blocks of 2048 words each is possible with the address scheme chosen.

As in the case of the ROM, the RAM when selected, places a word on the I-buss to be read and at the same time actuates the ready line. The RAM responds to an additional requirement defined by the computer; namely, a write cycle. This cycle is under computer control and is signaled by bits A_{14} and A_{15}. When these two lines are both low, (inverted from $A_{14} = A_{15} = 1$ at the computer), the cycle is a write cycle, and with the ready signal returned, the computer, in step T3 presents a word to the output latch U20 and U21 sheet SN 28. This word is written

on the RAM at the memory address decoded from bits A_0 - A_{13}. Actual entry into RAM occurs when the write strobe is issued in step T3. This strobe is delayed from the output latch strobe by 500 nanoseconds to allow for data to be settled at the input of the RAM prior to writing.

3. Hardware Multiply and Divide: For many applications, multiplication and division can be handled by software using addition, subtraction, and shift instructions. There are no multiply or divide instructions in the instruction set. Software multiplication and division are relatively slow, and if more speed is required, a hardware device, (HMD), increase speed very substantially. In the vapor detection system two 4 by 6 inch cards hold the necessary components for the HMD function. The HMD used is a conventional add-shift device which is operated from the computer as a set of memory locations. It is a synchronous to the computer, having its own clock. Mis-timing of data transfer is precluded by the use of the WAIT step in the computer cycle. The HMD issues a ready signal only after it is prepared for data transfer either in or out. In a typical utilization of the HMD, data are loaded, for the operands, to registers on the HMD board. The routing of these data for either multiplication or division is under address control through bits A_3, A_4, A_5; bit A_3 actually sets multiply or

divide routing by appropriate setting of the flip flop shown in sheet SN 32, U2 {1-6} .

A total of four bytes of operand data are entered by the computer 0-buss and routed by address decoding of A_o, A_1, A_2, in U19 along with the multiply/divide decoding held in U2. The operation cycle under HMD clock control is initiated with the entry of the fourth byte. Multiplication of 8 bit by 16 bit operands and division of 24 bit by 8 bit operands requires about 35 microseconds. The results, either product, or quotient and remainder, are held in the shift registers U8 - U13 of sheet SN 32. These are gated, under address control, 8 bits at a time through U15 - U20 to the I-buss for reading by the computer. The HMD ready line is not actuated until data are ready; however, since the computer must advance an address and call the data, the delay to the computer will be less than 20 microseconds.

4. Display: The output information from the vapor detection system is displayed with 256 step resolution on a conventional television set. In order to reduce the display load on the computer time, a display controller with its own memory is interposed between the computer and the vido system. This controller with its own independent clock supplies all of the video and synchronizing signals required for a static display. The computer communicates

with the display controller only when new data need to be displayed.

Since the display involves a video band width of about 4 MHz, a very fast memory must be used in its controller. The data for display are stored on a 32 word by 8 bit fast bipolar RAM. Since this RAM is continuously in use by the display, entries from the computer must be interlaced with the display RAM control cycle. To accomplish this without disturbing computer timing, address and data information from the computer for the controller is captured under computer control on latches in the controller. These latches are comprised of U18 - U21 shown on sheet SN 34. Data are then read from these latches into the fast memory, U9 - U12 with timing mediated by the display controller. This internal transfer is selected 16 times during each raster line, or about every 2.6 microseconds. The available time for transfer is approximately 200 nanoseconds in the interlace with video requirements. The internal transfer is inhibited during the time in which the computer writes on the latches by disabling of the gate at U16 {9} in order to avoid even a temporary ambiguity of data entry to the fast RAM.

From the standpoint of the computer, the display controller is simply a "write only memory" of 32 words. From the stand point of the system, it contains a memory which is shared

between the computer and the display with duplexed address control and completely asynchronous timing.

5. Spectrometer Interface: The normal spectrometer cycle time is approximately one millisecond. During this time, an elaborate sequence of events takes place. While these events could easily be placed under computer program control, use of the computer for sequence control would consume a great deal of computer time. For this reason, a hardware controller and interface have been provided for control and reading the spectrometer. This subsystem is divided into two sections which are interconnected via opto isolators to isolate the ground of the sensitive analog section from the rest of the system and thereby avoid ground loop problems. The simplified block diagram of the subsystem is shown in Figure 14, and the description of the elements follows.

a. Interface: The interface cards, (in case A), are attached directly to the A, I, and O-busses. They serve primarily to decode the address and act as a two way data shunt under control of the computer. Sheet SN 33 is a detailed circuit diagram of the two circuit boards. Decoding of the spectrometer addresses for write and read is accomplished on board A11. Spectrometer commands are transmitted under decoded address control to the spectrometer input isolator in case B. Two control words for

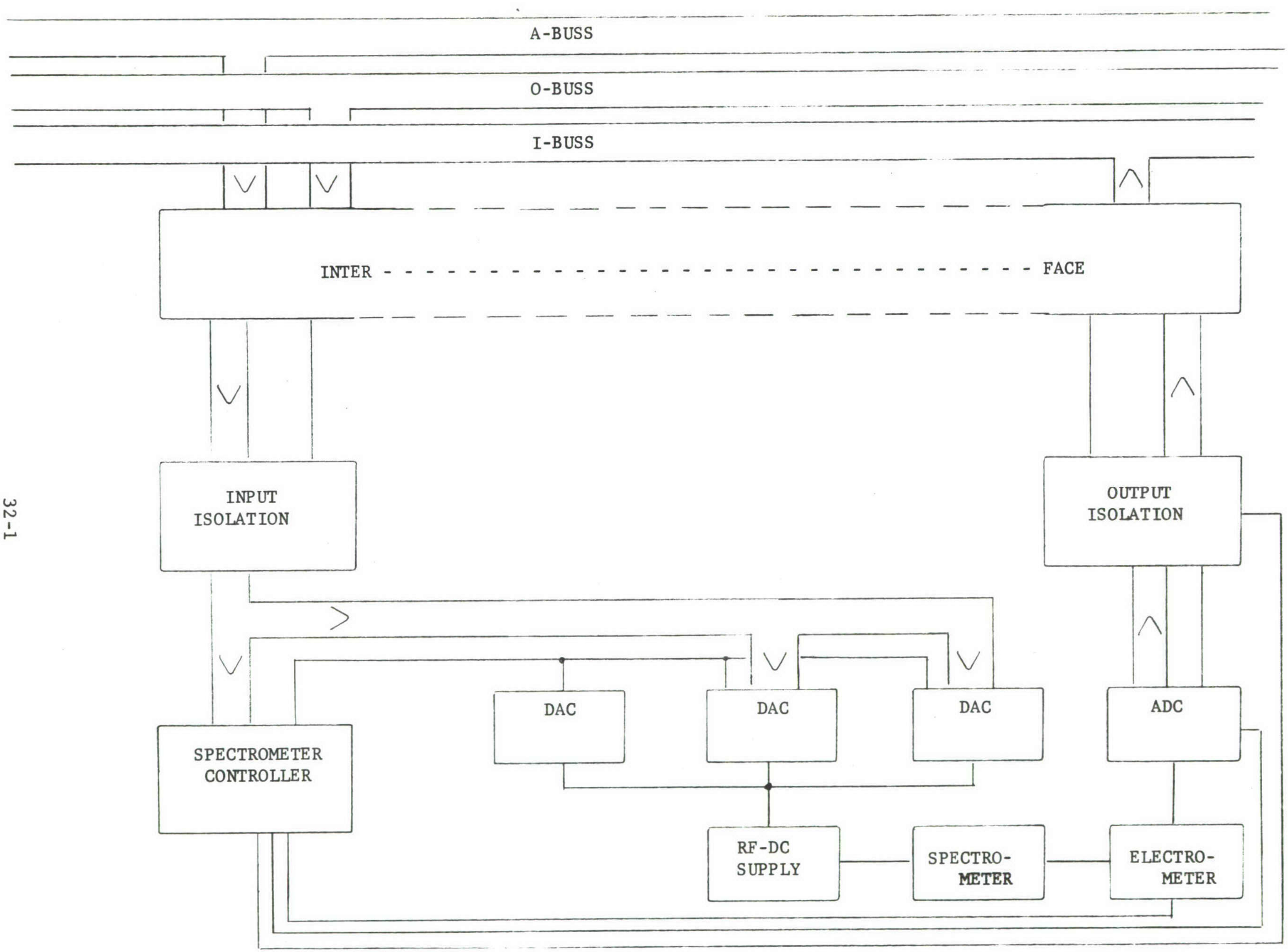


FIGURE 14.
Spectrometer Interface Scheme

mass selection and one dummy word to start the spectrometer controller are transmitted via the control and O-buss gates U15-U17.

Data are returned to the interface on card A10 from the spectrometer output isolator where they are stored at the end of a spectrometer cycle. Access to these data is under computer control to gate them on to the I-buss. The data are returned in two 8-bit bytes each byte being gated in response to a specific address. The gates and the computer ready signal cannot be actuated even with the proper address call until the controller has signaled "data ready" via U11 {10, 13} ,(sheet SN 33); thus assuring transmission of valid data to the computer.

b. Optical Isolation and Data Control: The data transmitted to and from the interface pass to the spectrometer input and output elements via opto isolators shown in sheets SN 14 and SN 15. Optical isolation is completely straight forward. The eleven lines used for spectrometer input are routed to two of the three DAC elements. One of these is on the same card as the spectrometer input isolator shown in sheet SN 14. Data, 8 bits at a time, are routed by a decoding of two control bits, (a_8 and a_9) and latched in the DAC's by the routed input strobe, (a_{10}).

Decoding and routing of the input strobe is carried out on the controller card.

The output isolator card, (see sheet SN 15) includes a duplexer, U15 and U16, to route the 16 bit digitized electrometer signal through the optoisolators to the output latches, U18-U21, in two 8 bit bytes. Routing is mediated by the spectrometer controllers, and the routing control signal and output strobe are themselves transmitted via optical isolators to direct the latching of data and actuation of the data ready line.

c. Spectrometer Controller: The function of this element is to sequence the various steps of spectrometer operation including the following items:

(1) load nominal mass DAC, (even masses)

(2) open electrometer integrate range sense

(3) load mass correction DAC

(4) start mass sweep steps and sweep DAC

(5) release electrometer integrate reset

(6) count mass sweep steps

(7) terminate electrometer range sensing

(8) initiate sample and hold

(9) initiate analog to digital conversion

(10) sense conversion complete

(11) reset electrometer integrator

(12) transmit first byte data

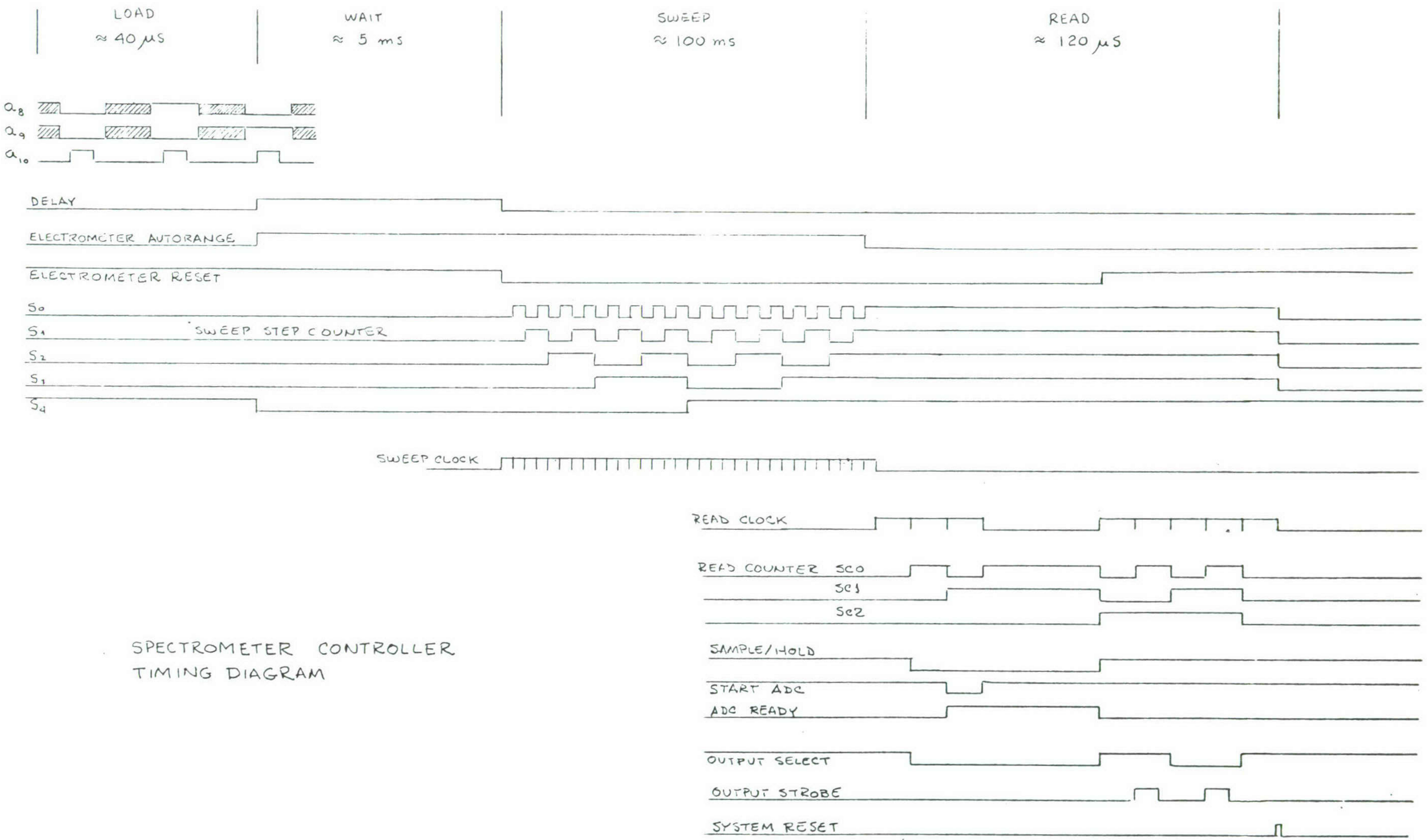
(13) transmit second byte data

(14) set data ready line

(15) go to idle.

A schematic of the controller is found in sheet SN 13. The controller starts in an idle condition with the clocks, U1, U7, U2, U3 silent. Initial sequencing occurs when a_8, a_9 and the strobe are actuated. Decoding of $a_8 = a_9 = 0$ will allow the strobe to pass to "gate mass"; $a_8 = 1$, $a_9 = 0$ with the strobe actuate "gate correction"; and $a_8 = 0$, $a_9 = 1$ with the strobe actuate "start". These events are shown at the upper left on the timing diagram given in Figure 15. The "start" signal also opens the electrometer integrate range sense in U5 {5} .

The "start" command initiates a 4 millisecond delay with U4 for spectrometer settling prior to sweep. At the end of the delay, the sweep stepping clock, U1 is released to start, and the electrometer integration reset is released by U5 {9}. The counters U17 and U10 count sweep steps from 0 to 31; the 5 coded count bits are available to the sweep DAC. At state 31, the electrometer integrate range sense is closed; (one state step of about 3 milliseconds before analog to digital conversion).



SPECTROMETER CONTROLLER
TIMING DIAGRAM

FIGURE 15

The completion of state 31 initiates the read sequence. The sweep step clock stops, and the reader clock U3 is started by U6 {12} . This clock steps the upper 3 bits of the counter U10. Whereas the mass step clock rate is about 3 milliseconds per pulse, the reader clock rate is about 10 microseconds per pulse. The second step of the reader clock sets the sample and hold command; the third initiates the electrometer ADC conversion. During the conversion which occupies about 30 microseconds, the reader clock is held up by the end conversion line via U6 {13, 12} . When conversion is complete, the reader clock recommences. The fourth reader clock pulse sets the duplex for the first byte of ADC data and the fifth strobes this byte to the spectrometer output data latches. The sixth pulse sets the duplex for the second byte of data, and the seventh strobes this second byte to the second set of output data batches. The last reader clock pulse spaces a general reset pulse which resets the state counters through U19 {13} and U8 {3, 6} . At this point the controller has completed its cycle and is ready for the next command.

III SOFTWARE

A. GENERAL DESCRIPTION

1. Structure: The Intel 8008 microprocessor used in the suitcase computer is byte oriented and has a generous (8 level) address stack. These features, combined with the large variety of operations and data processing required, prescribe a program for operation of the spectrometer and its data processing and display which is heavily built on the use of subroutines, many of which are used for multiple purposes.

Since the permanent program is stored on (reprogrammable) read only memory (ROM), no special provision is required to save memory at shutdown. The shutdown cycle is simply the removal of power to the system and every restart performs a complete initialization. There are no requirements to complete any instruction loop at shutdown.

The memory used in the program is comprised of 1792 words of ROM and 1024 words of random access memory (RAM). The RAM is volatile and is lost upon power shutdown.

All of the routines used in the program are called from a primary operation loop (PLOP) located at the beginning of the ROM, and each subsidiary loop returns eventually to the primary loop.

The direction of the program from the primary loop is governed by operator selection of front panel switches. Each subsidiary loop will continue to its normal terminus before the program will accept the direction of new switch commands.

Movable instructions and data are handled in the RAM. Address organization in the RAM is designed to reduce the manipulation required to generate two word memory addressing. The principal organization of the RAM for data handling is built around a data matrix of 8 columns by 32 rows. This matrix organizes the storage of raw and processed data from the inspection of up to 16 mass peaks in double precision. A matrix address director routine (MADD) maneuvers the program operations through this matrix.

2. Operations: The program provides for the ordering and execution of four principal operations described below.

a) Start-up and executive loop: When power is applied to the system, an interrupt command applied from the front panel through the computer reset switch starts the program. This operation first initializes the RAM and then proceeds to the primary loop (PLOP).

b) Read the switches: The program is under operator control through the front panel switches. These switches are monitored in the primary loop and in every subsidiary loop. The computer

interprets the switch commands, and each interpretation accesses one or more subsidiary loop to direct the system operation.

c) Control of hardware: Peripheral hardware is operated by the computer and data are returned in the case of the spectrometer. The program accesses the peripherals simply as memory locations with either write or read properties. There are three peripheral hardware elements; namely, the spectrometer, the display, and the hardware multiply and divide.

From the point of view of the program, the spectrometer is a five word memory; three words for writing and two words for reading. The usual routine for the computer is to write three words for the command to the spectrometer to access a (half) peak segment. The actual scanning of the half peak segment is performed by an independent digital hardware controller in a normal time of approximately 50 milliseconds. Data are captured in a two word memory and are ready for access when required. During the time of operation of the spectrometer, the computer is free to perform other functions such as data processing. No interrupts are used; when the computer is ready for data it simply accesses the two word memory where data are held. A valid data ready signal is included in this access cycle to prevent the transmission of faulty data.

The computer accesses the display as a "write only memory" of 32 words, each word representing one vertical bar on the display screen. Data written into this memory are used continuously by the hardware display controller, and the display continues indefinitely without mediation of the computer. Rapid update of the display one word at a time can be called from the computer; however, the computer is completely free of any tasks of display operation.

The instruction set of the Intel 8008 does not include multiply and divide instructions. Since in the CPU these processes, if carried out by program or micro-program control would be extremely time consuming, a fast hardware multiply and divide element is included in the computer. This element is structured to handle 3 byte 24 bit results. Its access is through four address locations to enter operands each for multiply and divide and three address locations each to quotient and product results.

d) Data processing: The nominal fragment ion mass values are prescribed in the mass table along with software gain factors to be used in data processing. The primary data handling and processing accesses major manipulations, including the data matrix mentioned above, a data scaling routine using a software gain control, an exponential filtering routine, a square root data compression routine, and sweep calibration routines.

The data scaling routine applies a software gain factor to the spectrometer data which arrive with 10 bit resolution and octal exponent scale factors designed to rationalize data from all peaks, (which may vary in intensity by factors larger than 10^4), into a 16 bit format. The dynamic range of the software gain control is 11 bits and that of the electrometer is 19 bits. Prior knowledge of the background spectrum and signature peak ratios is used to set the software gain factors. Overrange provision is made for peaks which may fall outside the dynamic capacity of the data scaling process.

The exponential filter successively applies a smoothing routine to the data for each peak, using a variety of time constants. The basic algorithm used successively from column to column in the data matrix is as follows:

$$P_{k,\ell}^{(o)} = A\left[P_{(k-1),\ \ell}\right] + (1 - A)\left[P_{k,\ell}^{(1)}\right] \tag{1}$$

where the superscript (o) refers to the current value and (1) refers to the next prior value, ℓ refers to the row in the matrix for a particular fragment ion mass, and k is the column index and the sequence of smoothing. Analog expressions for (1) may be stated as follows:

$$X_{1,\ell}(t) = \frac{1}{\tau_1}\int_{-\infty}^{t} e^{\frac{t'-t}{\tau_1}} X_{o,\ell}(t')\,dt' \qquad (2),$$

$$X_{2,\ell}(t) = \frac{1}{\tau_2}\int_{-\infty}^{t} e^{\frac{t'-t}{\tau_2}} X_{1,\ell}(t')\,dt' \qquad (3),$$

$$X_{3,\ell}(t) = \frac{1}{\tau_3}\int_{-\infty}^{t} e^{\frac{t'-t}{\tau_3}} X_{2,\ell}(t')\,dt' \qquad (4),$$

and (2), (3), and (4) may be combined to give

$$X_{2,\ell}(t) = \frac{1}{\tau_2}\int_{-\infty}^{t} e^{\frac{t'-t}{\tau_2}} \frac{dt'}{\tau_2} \int_{-\infty}^{t'} e^{\frac{t''-t}{\tau_1}} X_{o,\ell}(t'')dt'' \qquad (5),$$

$$X_{3,\ell}(t) = \frac{1}{\tau_3}\int_{-\infty}^{t} e^{\frac{t'-t}{\tau_3}} \frac{dt'}{\tau_2} \int_{-\infty}^{t'} e^{\frac{t''-t'}{\tau_2}} \frac{dt''}{\tau_1} \int_{-\infty}^{t''} e^{\frac{t'''-t''}{\tau_1}} X_{o,\ell}(t''')\,dt''' \qquad (6),$$

In equations (2) - (6), $X_{1,\ell}$, $X_{2,\ell}$ and $X_{3,\ell}$ are the successively smoothed values of the input data $X_{o,\ell}$, and τ_1, τ_2, and τ_3 are the respective smoothing time constants.

The square root routine generates a close approximation to the true square root of 16 bit data values, thereby reducing the span of the data values to 8 bits for the display without loss of sensitivity in the display to the eye for small peaks. The square root is

generated by computing the binary logarithm of the number approximately, in one step, dividing this logarithm by two, and then computing the antilogarithm of the quotient approximately again in one step. This compact program produces errors which are small and progress smoothly on the high side of true values between the numbers which are squares of integers. Roots of the squares of integers are computed exactly.

The computation is carried out as follows: If N is a binary number ≥ 1 expressed as

$$N = 2^k + R$$

where $R = a_1 \, 2^{k-1} + a_2 \, 2^{k-2} + \ldots$

and the a's are zero or one, the approximate binary logarithm is given by

$$\log_2 (2^k + R) \cong L_2 = (k - 1) + 2\left(\frac{R}{2^k} - \frac{a_1}{2}\right)$$

$$\text{or} \qquad L_2 = (k - 1) + M \tag{7}$$

To find the anti logarithm of $\frac{L_2}{2} = C + F$

where C is an integer and F is the remaining binary fraction, a similar approximation leads to $\sqrt{N}$:

$$\sqrt{N} \cong \text{antilog } (C + F) \cong 2^C \left\{ \tfrac{1}{2} (F + 1) \right\} \tag{8}$$

Where negative numbers are manipulated, the program is structured to give

$$\text{SQRT}\ (N < o) = -\text{SQRT}\ (|N|) \tag{9}$$

since the process is for data compression and not for mathematical function.

Sweep calibration is accomplished by comparing the intensity values for the (nominal) lower and upper half peaks addressed in the calibration routines. If the two half peak values are not equal, then the (DAC) value given the spectrometer for the peak was incorrect. If the lower half peak is the larger, then the (DAC) value is too high, and vice versa.

The DAC values are derived in the computer from the nominal value for the peak and a correction term which is interpolated for the peak from a correction table maintained in the RAM. In mode zero selected correction constants in this table are automatically adjusted until the two half peaks balance. In mode 7, adjustment of correction constants is under manual control.

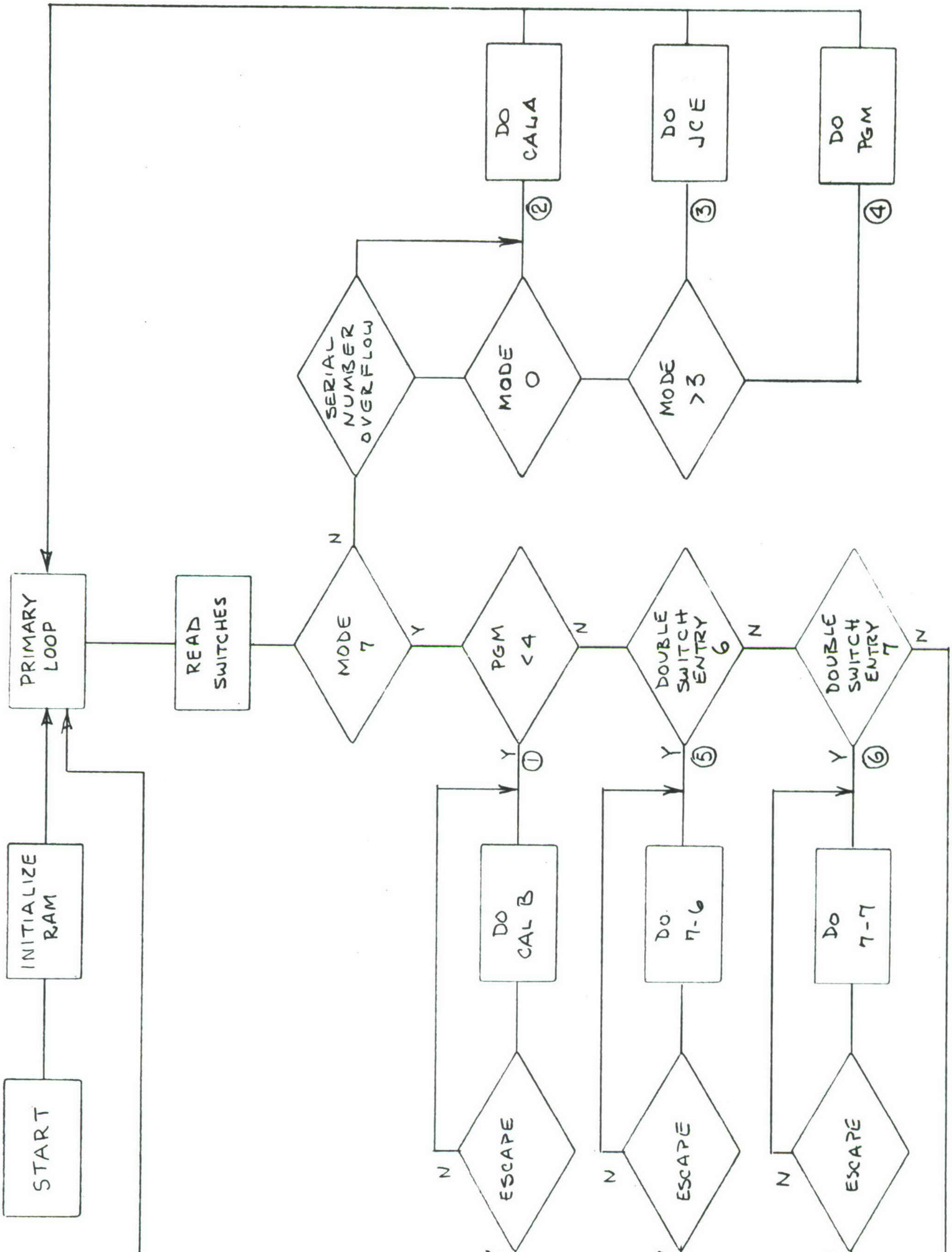
B. FLOW CHARTS

The flow charts attached outline the logic of various routines in the program. The first sheet shows the entry to the program and the operation of the primary loop. Numbers and letters appearing by the boxes refer to subsidiary routines on following sheets. There are many shorter routines in the call list pages following the flow charts. The functions of these routines is self evident and they may

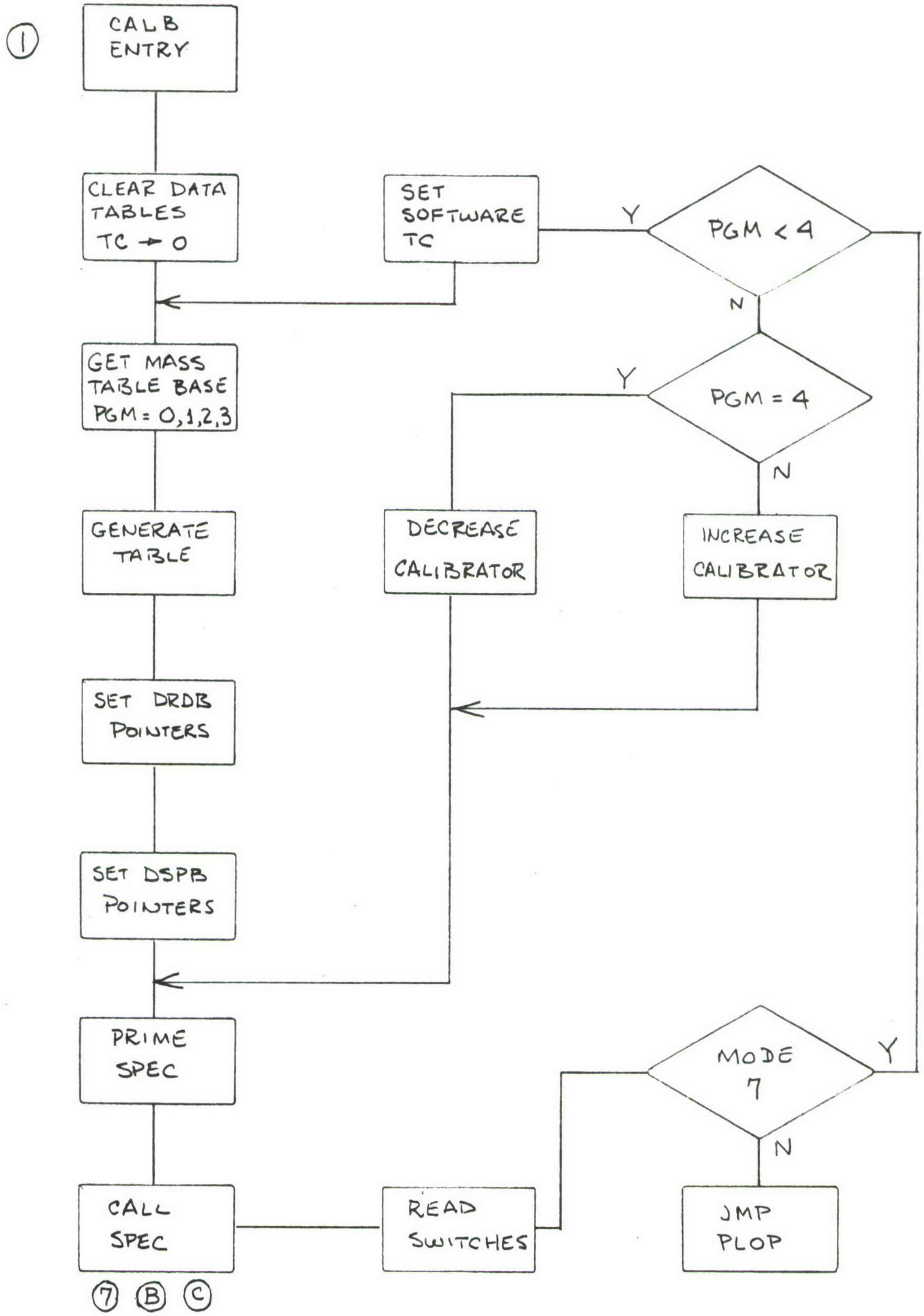
be traced easily in the listing.

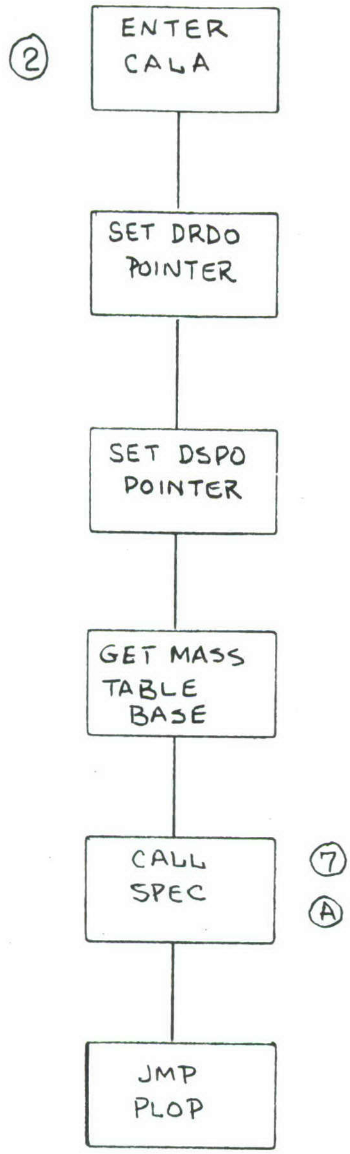
C. PROGRAM LISTS

1. Subroutine call list.
2. Memory maps.
3. Programmed mass table.
4. Double switch mass selection.
5. Program listing.

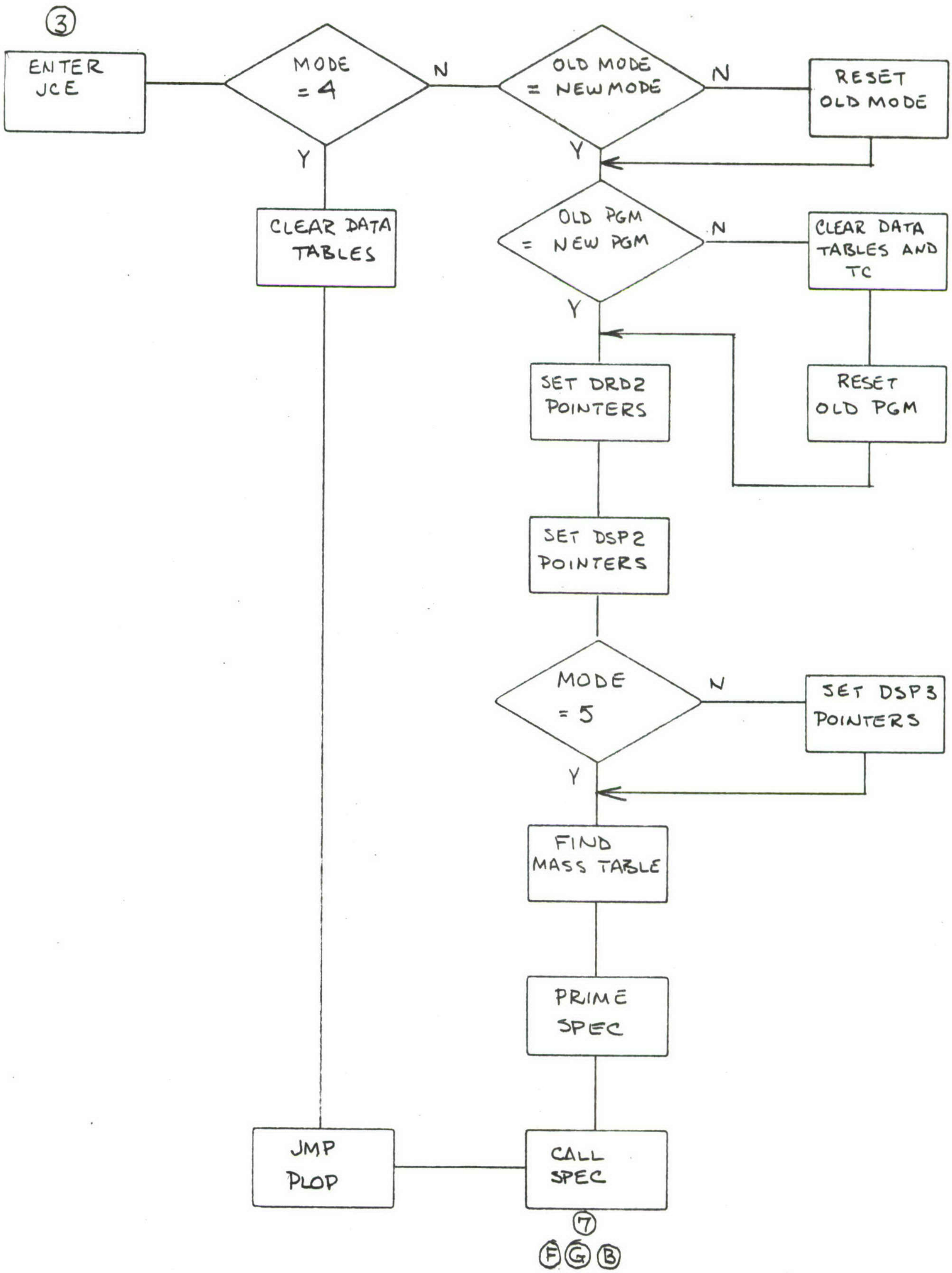


PRIMARY LOOP

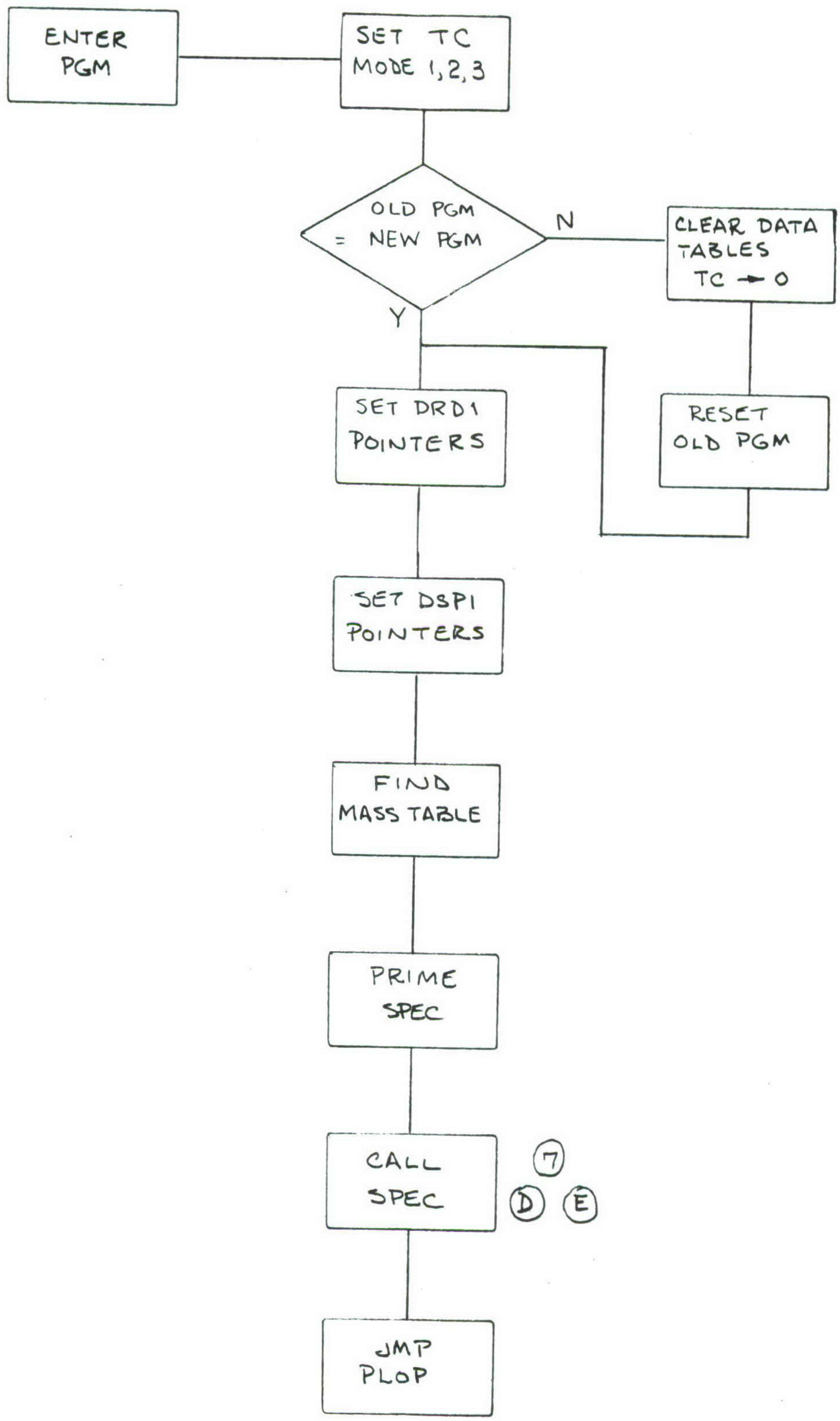

①
CALB ENTRY
CLEAR DATA TABLES TC → 0
SET SOFTWARE TC
Y
PGM < 4
N
GET MASS TABLE BASE PGM = 0,1,2,3
Y
PGM = 4
N
GENERATE TABLE
DECREASE CALIBRATOR
INCREASE CALIBRATOR
SET DRDB POINTERS
SET DSPB POINTERS
PRIME SPEC
MODE 7
Y
N
CALL SPEC
READ SWITCHES
JMP PLOP
⑦ Ⓑ Ⓒ

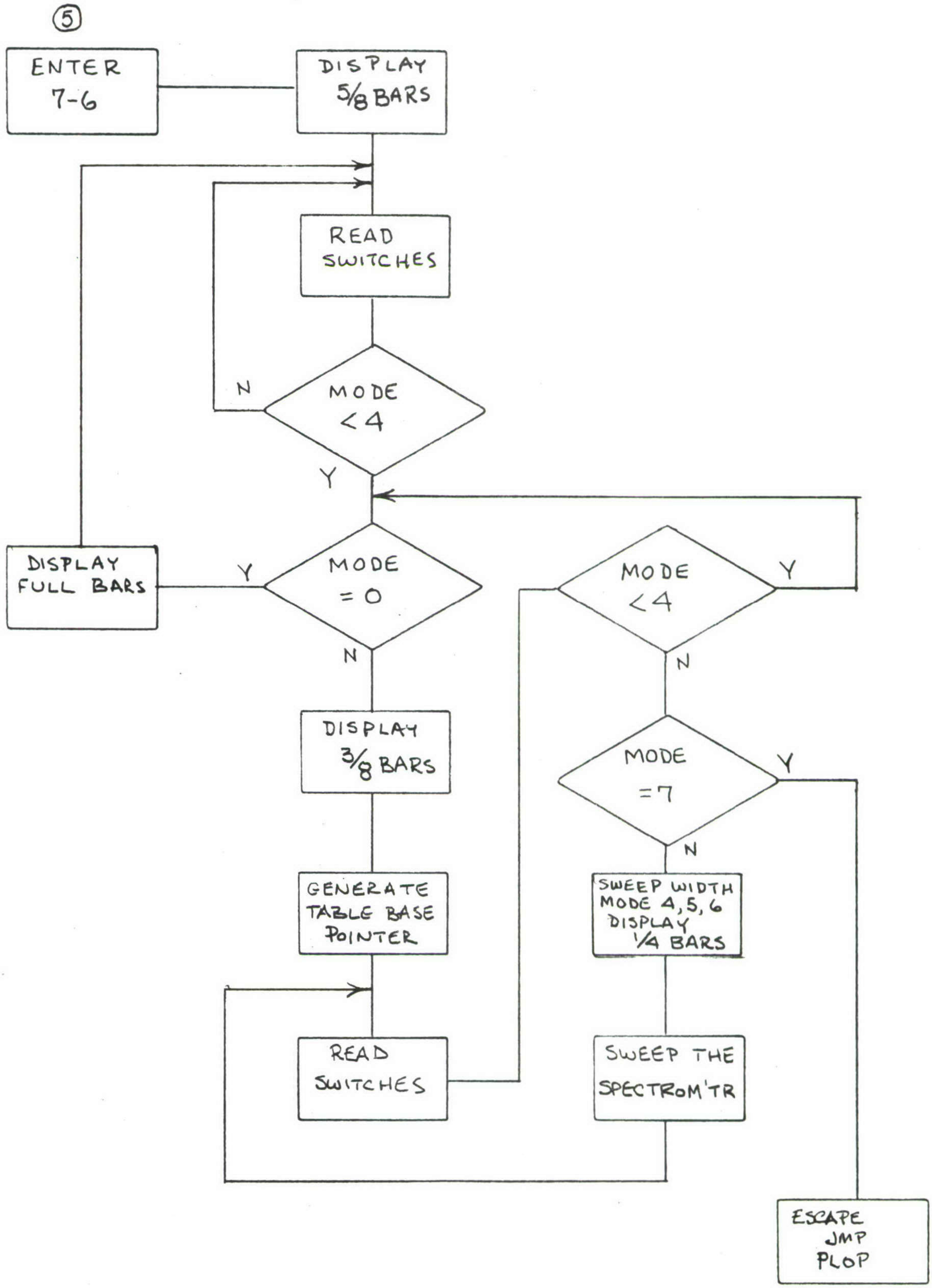

2
ENTER
CALA
SET DRDO
POINTER
SET DSPO
POINTER
GET MASS
TABLE
BASE
CALL
SPEC
7
A
JMP
PLOP

③ JCE

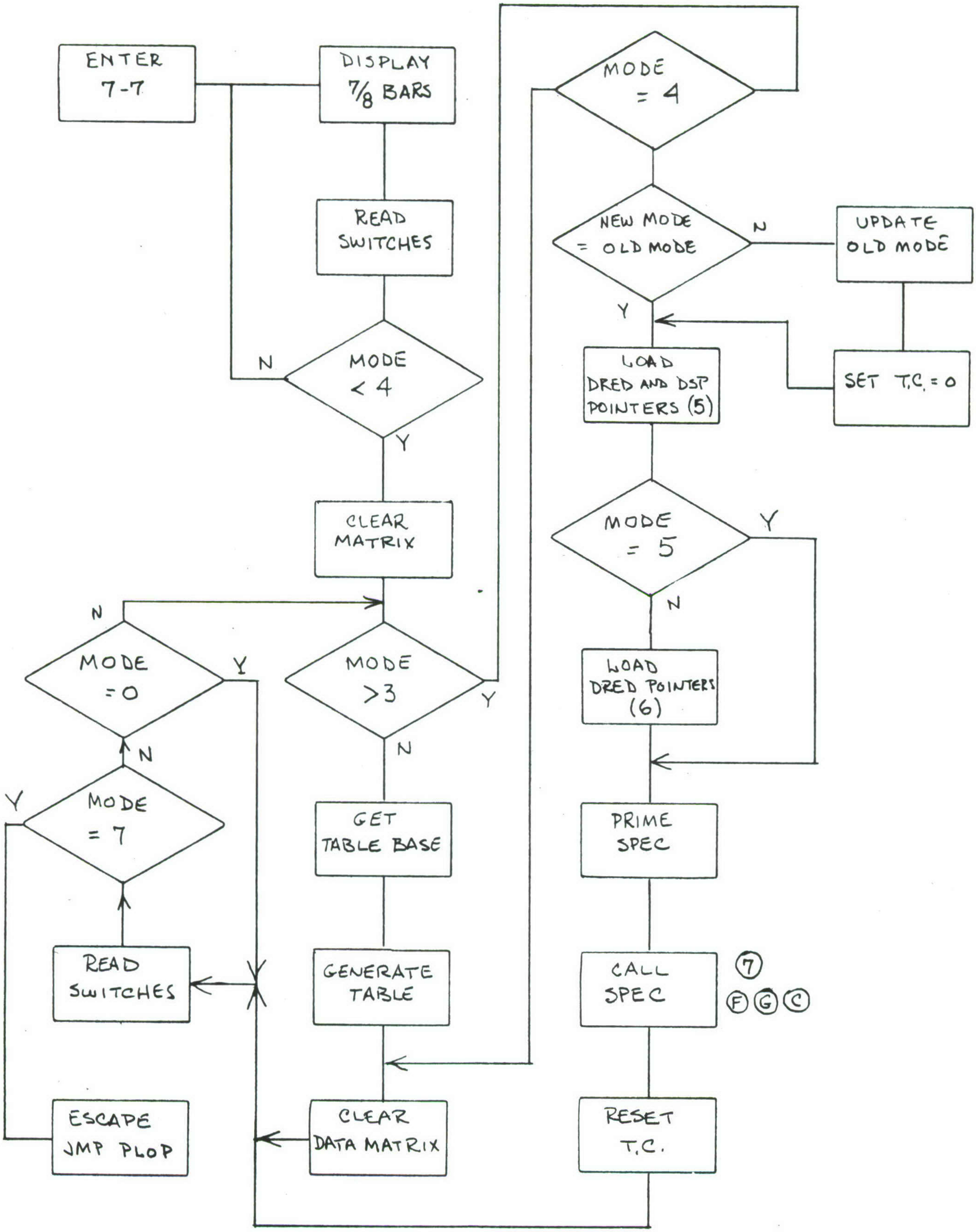

③
ENTER JCE
MODE = 4
N
Y
CLEAR DATA TABLES
OLD MODE = NEWMODE
N
Y
RESET OLD MODE
OLD PGM = NEW PGM
N
Y
CLEAR DATA TABLES AND TC
RESET OLD PGM
SET DRD2 POINTERS
SET DSP2 POINTERS
MODE = 5
N
Y
SET DSP3 POINTERS
FIND MASS TABLE
PRIME SPEC
JMP PLOP
CALL SPEC
⑦
Ⓕ Ⓖ Ⓑ

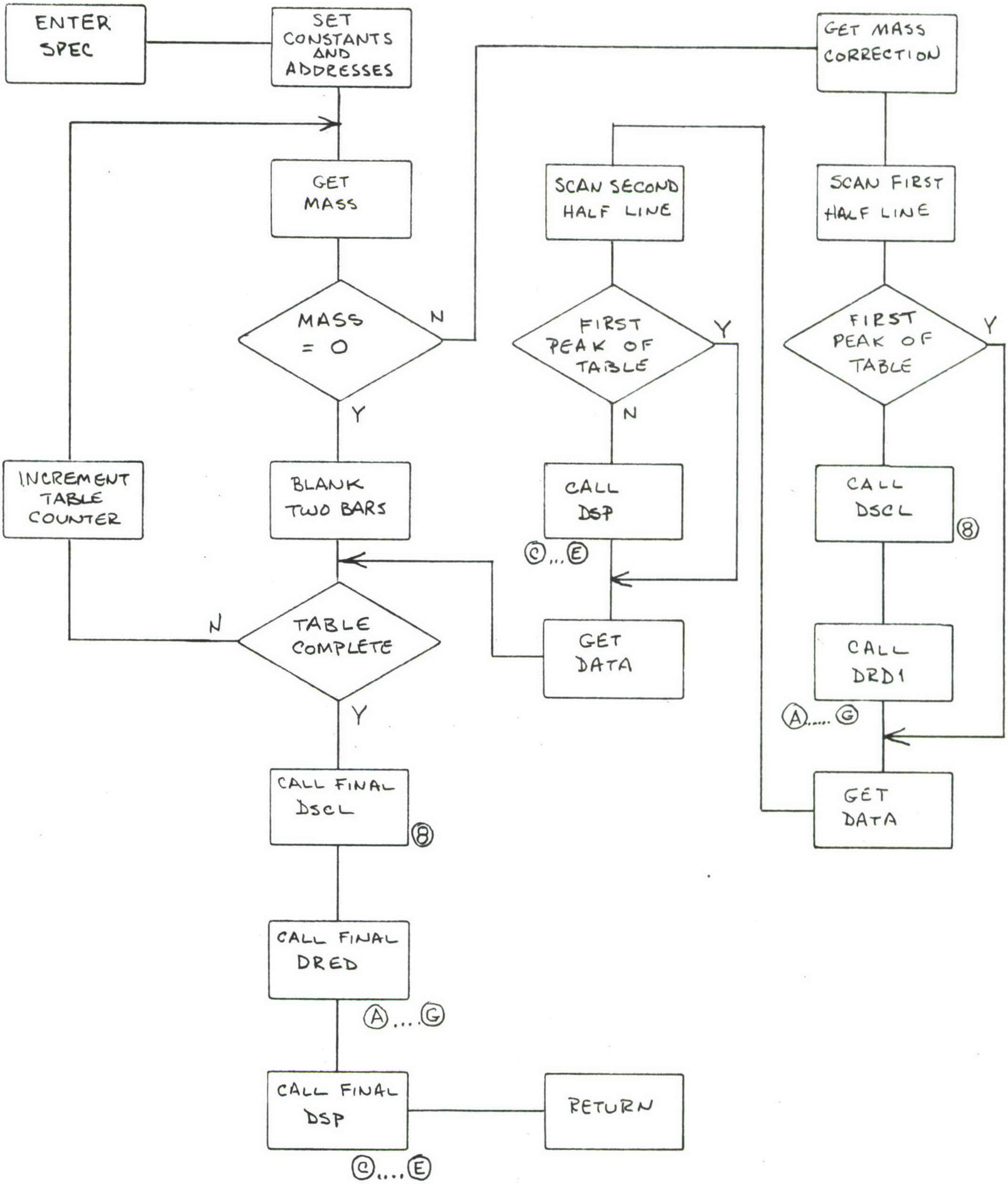
④ PGM


ENTER PGM
SET TC MODE 1,2,3
OLD PGM = NEW PGM
N
Y
CLEAR DATA TABLES TC → 0
RESET OLD PGM
SET DRD1 POINTERS
SET DSP1 POINTERS
FIND MASS TABLE
PRIME SPEC
CALL SPEC
7
D
E
JMP PLOP

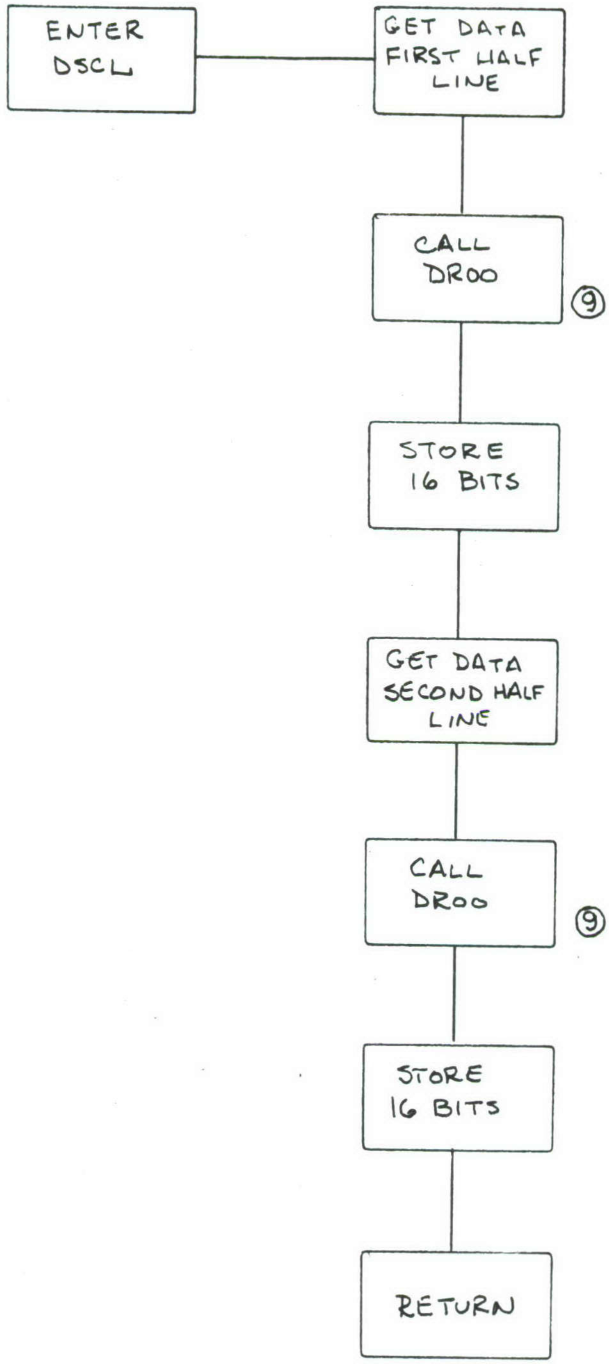

⑤
ENTER 7-6
DISPLAY 5/8 BARS
READ SWITCHES
MODE <4
N
Y
DISPLAY FULL BARS
MODE =0
Y
N
DISPLAY 3/8 BARS
GENERATE TABLE BASE POINTER
READ SWITCHES
MODE <4
Y
N
MODE =7
Y
N
SWEEP WIDTH MODE 4,5,6 DISPLAY 1/4 BARS
SWEEP THE SPECTROM'TR
ESCAPE JMP PLOP

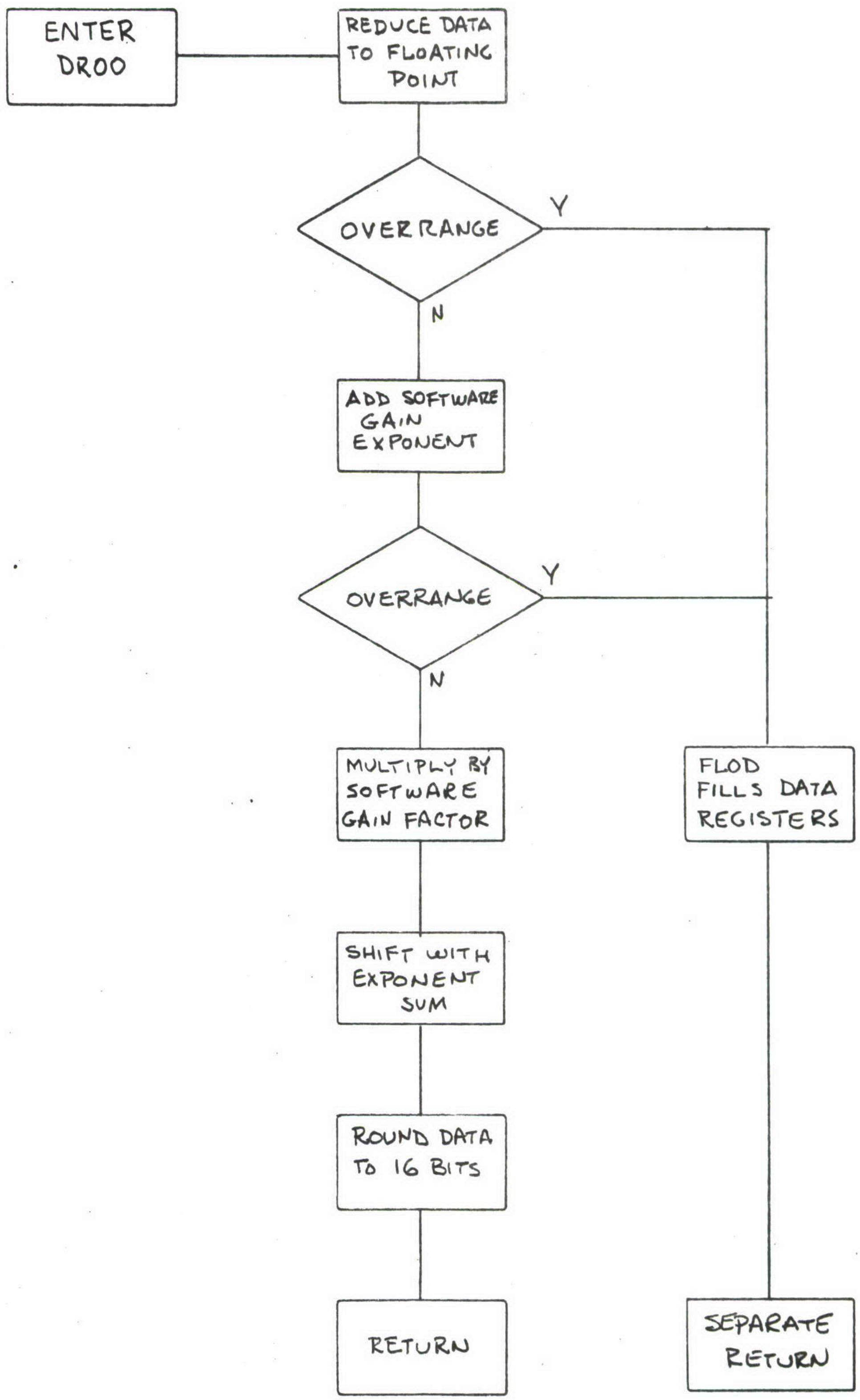
⑥ 7-7 SELECT

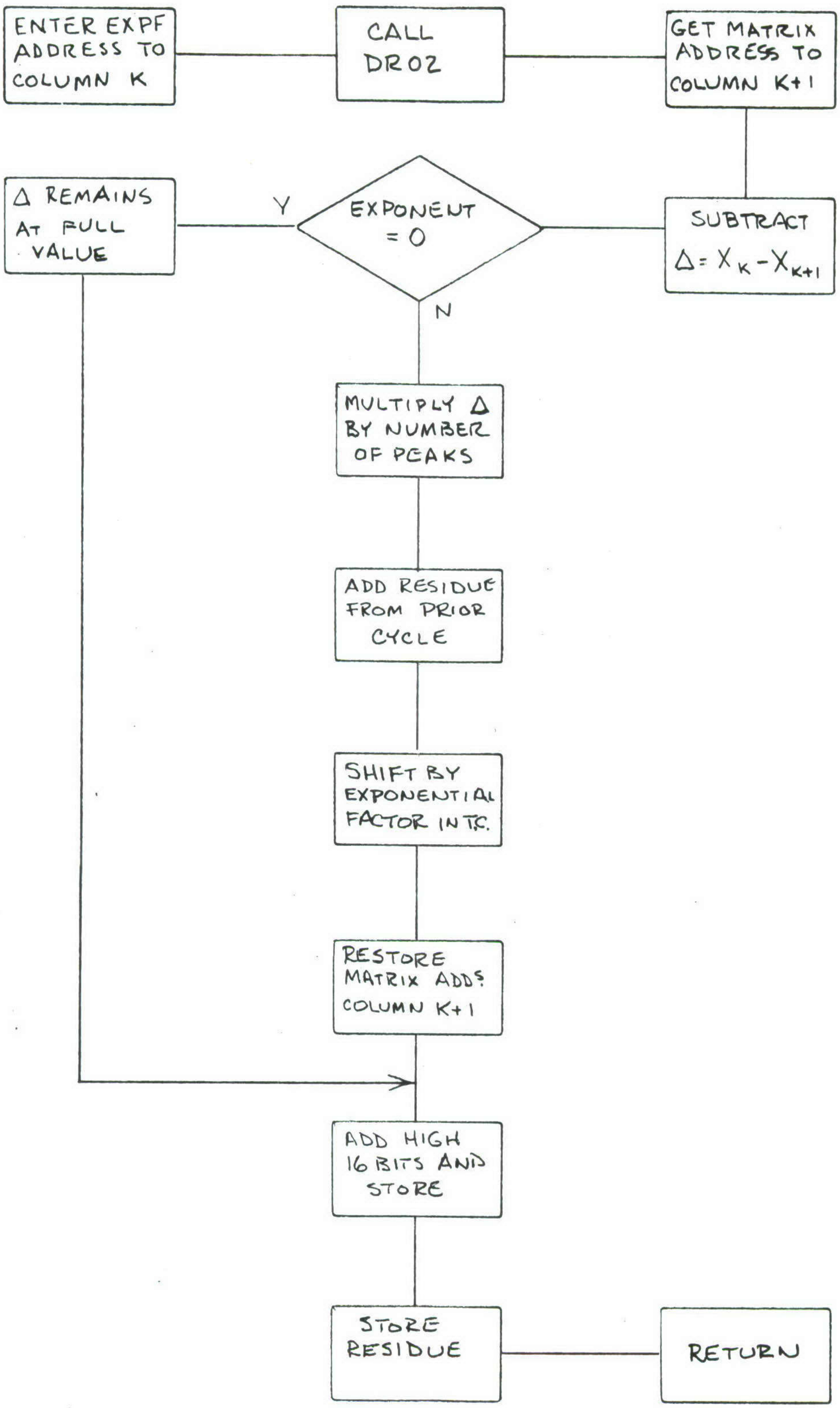

ENTER 7-7
DISPLAY 7/8 BARS
READ SWITCHES
MODE < 4
N
Y
CLEAR MATRIX
MODE > 3
Y
N
GET TABLE BASE
GENERATE TABLE
CLEAR DATA MATRIX
MODE = 0
Y
N
MODE = 7
Y
N
READ SWITCHES
ESCAPE JMP PLOP
MODE = 4
NEW MODE = OLD MODE
N
Y
UPDATE OLD MODE
SET T.C. = 0
LOAD DRED AND DSP POINTERS (5)
MODE = 5
Y
N
LOAD DRED POINTERS (6)
PRIME SPEC
CALL SPEC
⑦
Ⓕ Ⓖ Ⓒ
RESET T.C.


ENTER SPEC
SET CONSTANTS AND ADDRESSES
GET MASS
MASS = 0
N
Y
BLANK TWO BARS
TABLE COMPLETE
N
Y
INCREMENT TABLE COUNTER
CALL FINAL DSCL
8
CALL FINAL DRED
A.... G
CALL FINAL DSP
C.... E
RETURN
GET MASS CORRECTION
SCAN FIRST HALF LINE
FIRST PEAK OF TABLE
Y
CALL DSCL
8
CALL DRD1
A..... G
GET DATA
SCAN SECOND HALF LINE
FIRST PEAK OF TABLE
Y
N
CALL DSP
C... E
GET DATA

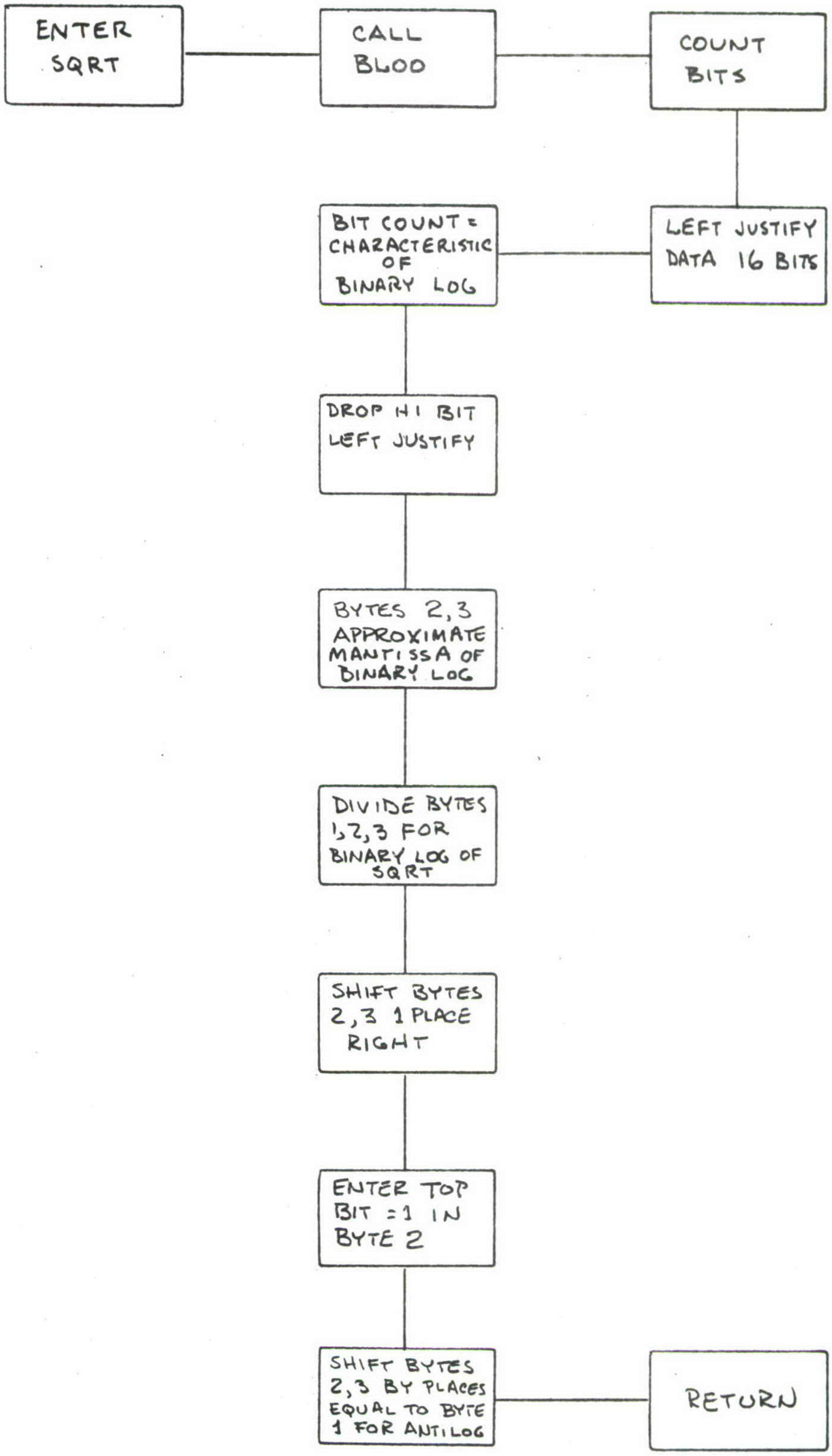
⑧ DSCL


ENTER DSCL
GET DATA FIRST HALF LINE
CALL DR00
⑨
STORE 16 BITS
GET DATA SECOND HALF LINE
CALL DR00
⑨
STORE 16 BITS
RETURN

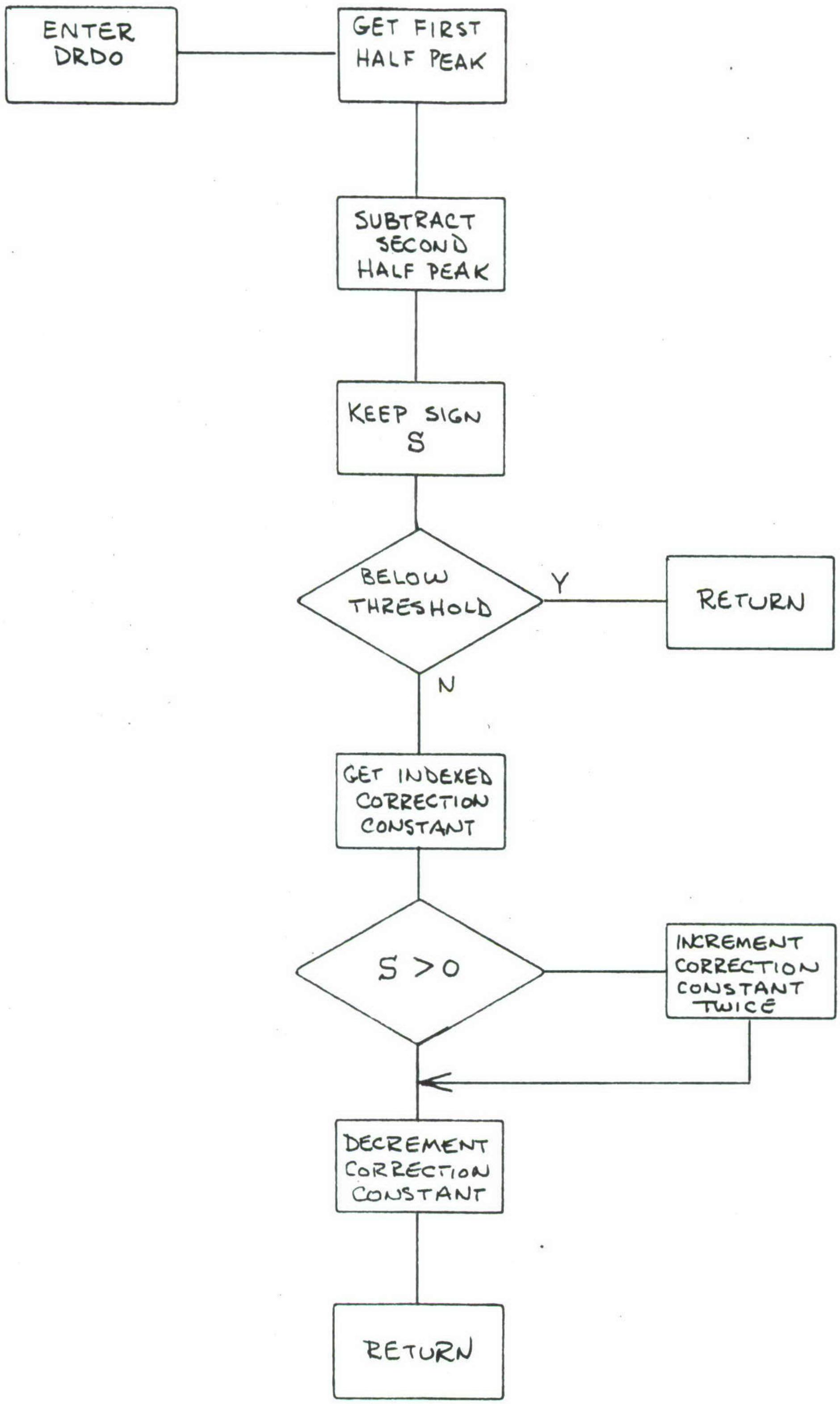

ENTER DROO
REDUCE DATA TO FLOATING POINT
OVERRANGE
Y
N
ADD SOFTWARE GAIN EXPONENT
OVERRANGE
Y
N
MULTIPLY BY SOFTWARE GAIN FACTOR
SHIFT WITH EXPONENT SUM
ROUND DATA TO 16 BITS
RETURN
FLOD FILLS DATA REGISTERS
SEPARATE RETURN



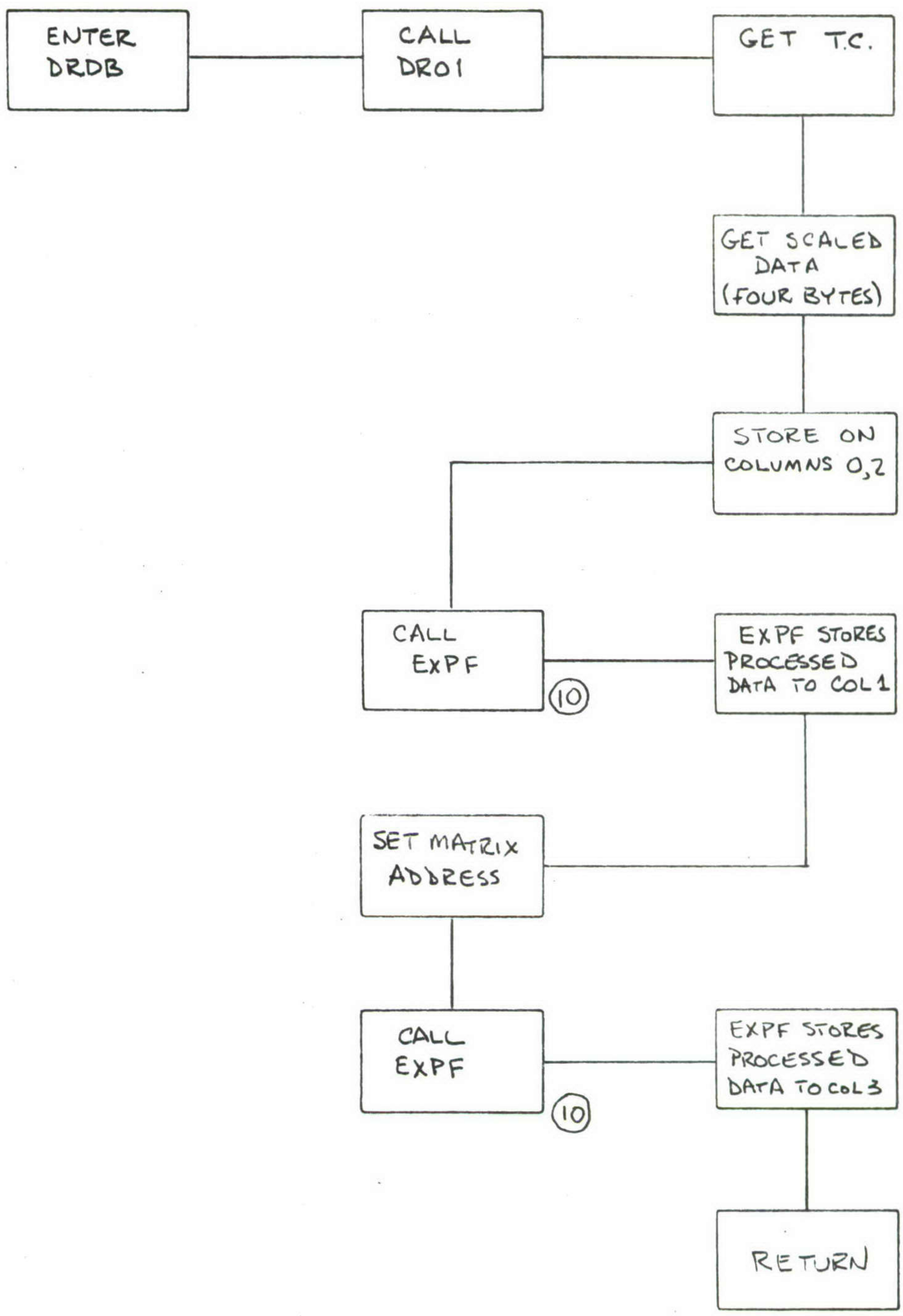
ENTER EXPF ADDRESS TO COLUMN K
CALL DR02
GET MATRIX ADDRESS TO COLUMN K+1
SUBTRACT $\Delta = X_K - X_{K+1}$
EXPONENT = 0
Y
N
Δ REMAINS AT FULL VALUE
MULTIPLY Δ BY NUMBER OF PEAKS
ADD RESIDUE FROM PRIOR CYCLE
SHIFT BY EXPONENTIAL FACTOR IN T.C.
RESTORE MATRIX ADDS COLUMN K+1
ADD HIGH 16 BITS AND STORE
STORE RESIDUE
RETURN


ENTER SQRT
CALL BLOO
COUNT BITS
LEFT JUSTIFY DATA 16 BITS
BIT COUNT = CHARACTERISTIC OF BINARY LOG
DROP HI BIT LEFT JUSTIFY
BYTES 2,3 APPROXIMATE MANTISSA OF BINARY LOG
DIVIDE BYTES 1,2,3 FOR BINARY LOG OF SQRT
SHIFT BYTES 2,3 1 PLACE RIGHT
ENTER TOP BIT =1 IN BYTE 2
SHIFT BYTES 2,3 BY PLACES EQUAL TO BYTE 1 FOR ANTILOG
RETURN

Ⓐ DRDO

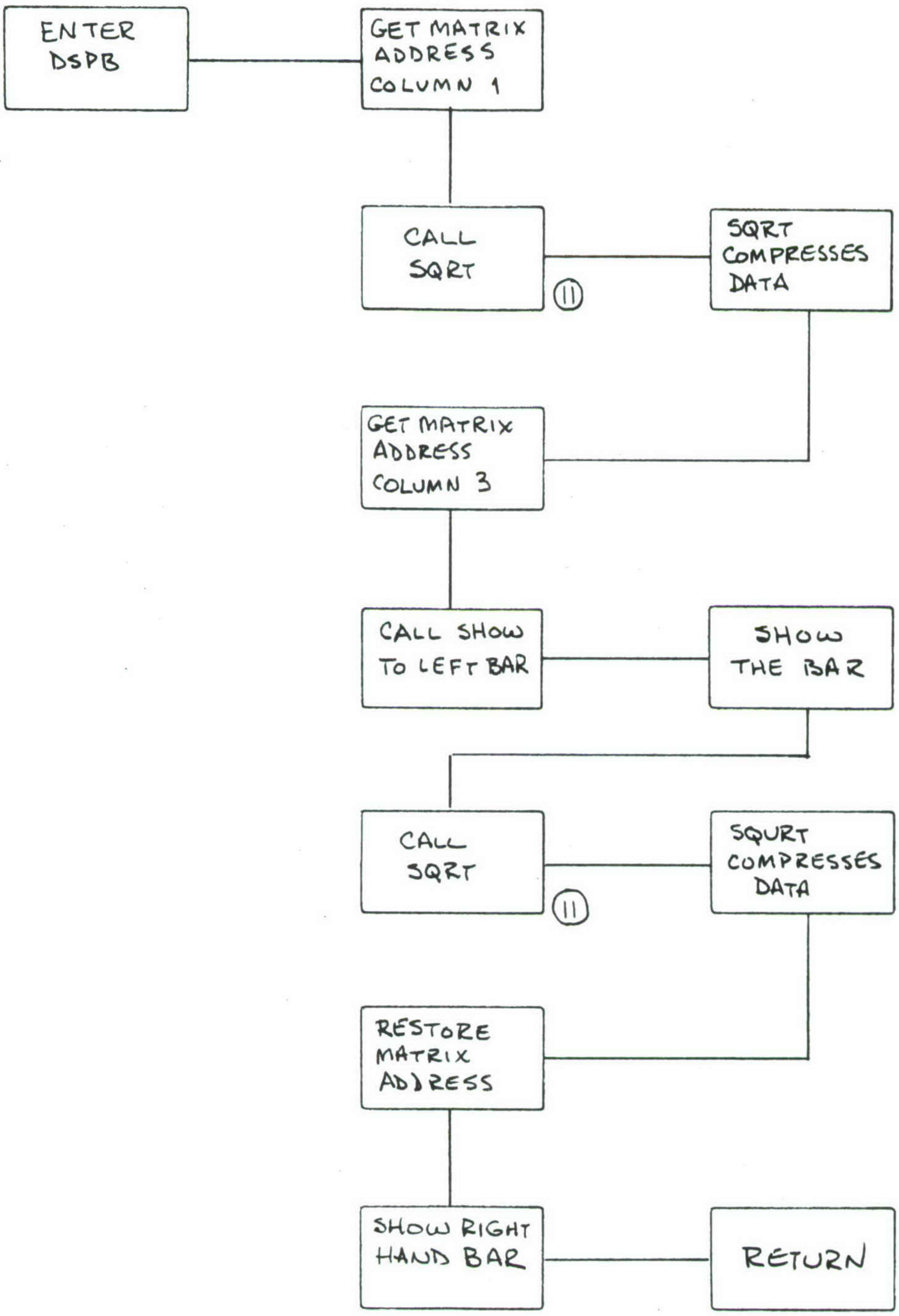

ENTER DRDO
GET FIRST HALF PEAK
SUBTRACT SECOND HALF PEAK
KEEP SIGN S
BELOW THRESHOLD
Y
RETURN
N
GET INDEXED CORRECTION CONSTANT
S > 0
INCREMENT CORRECTION CONSTANT TWICE
DECREMENT CORRECTION CONSTANT
RETURN

Ⓑ DRDB

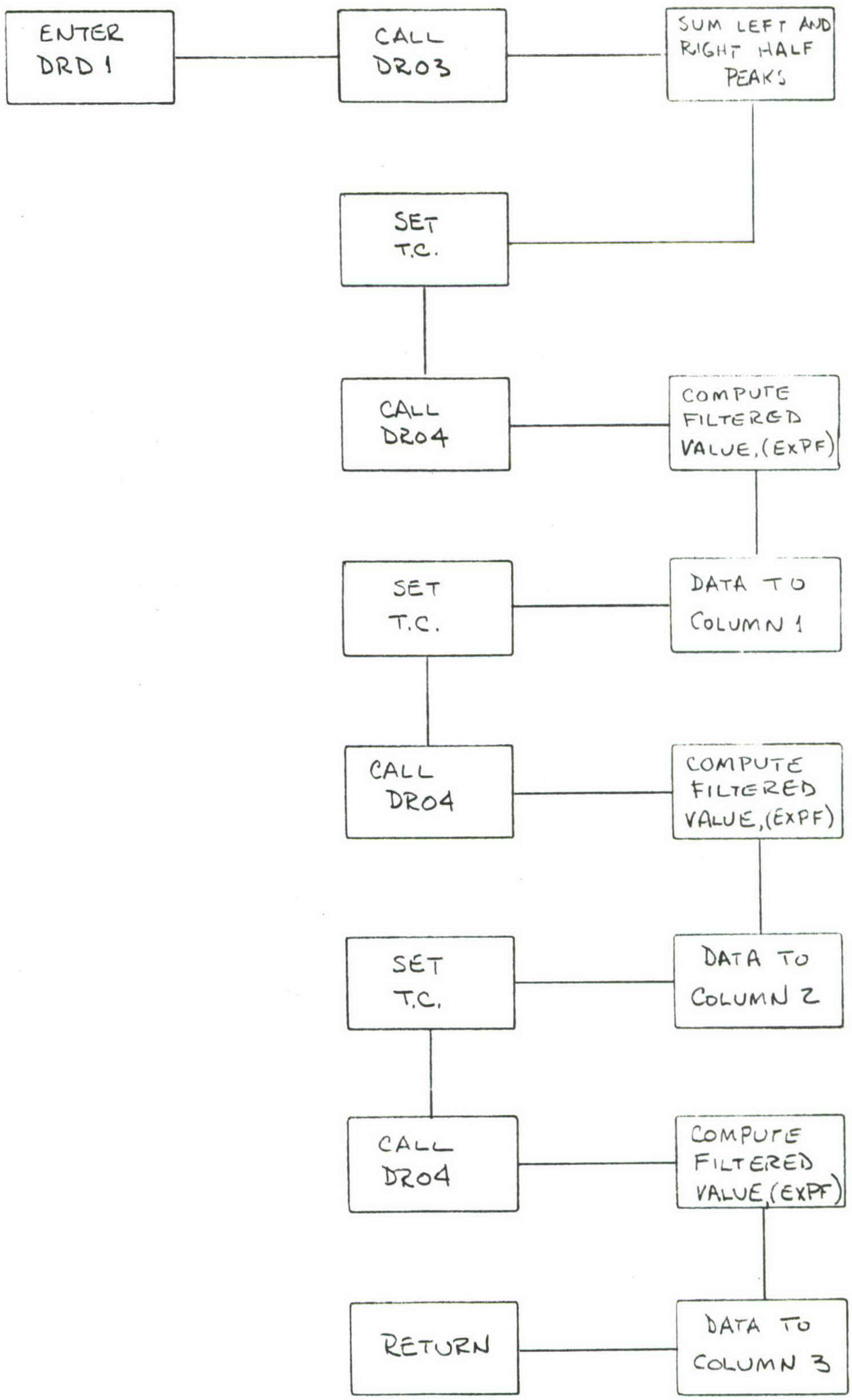


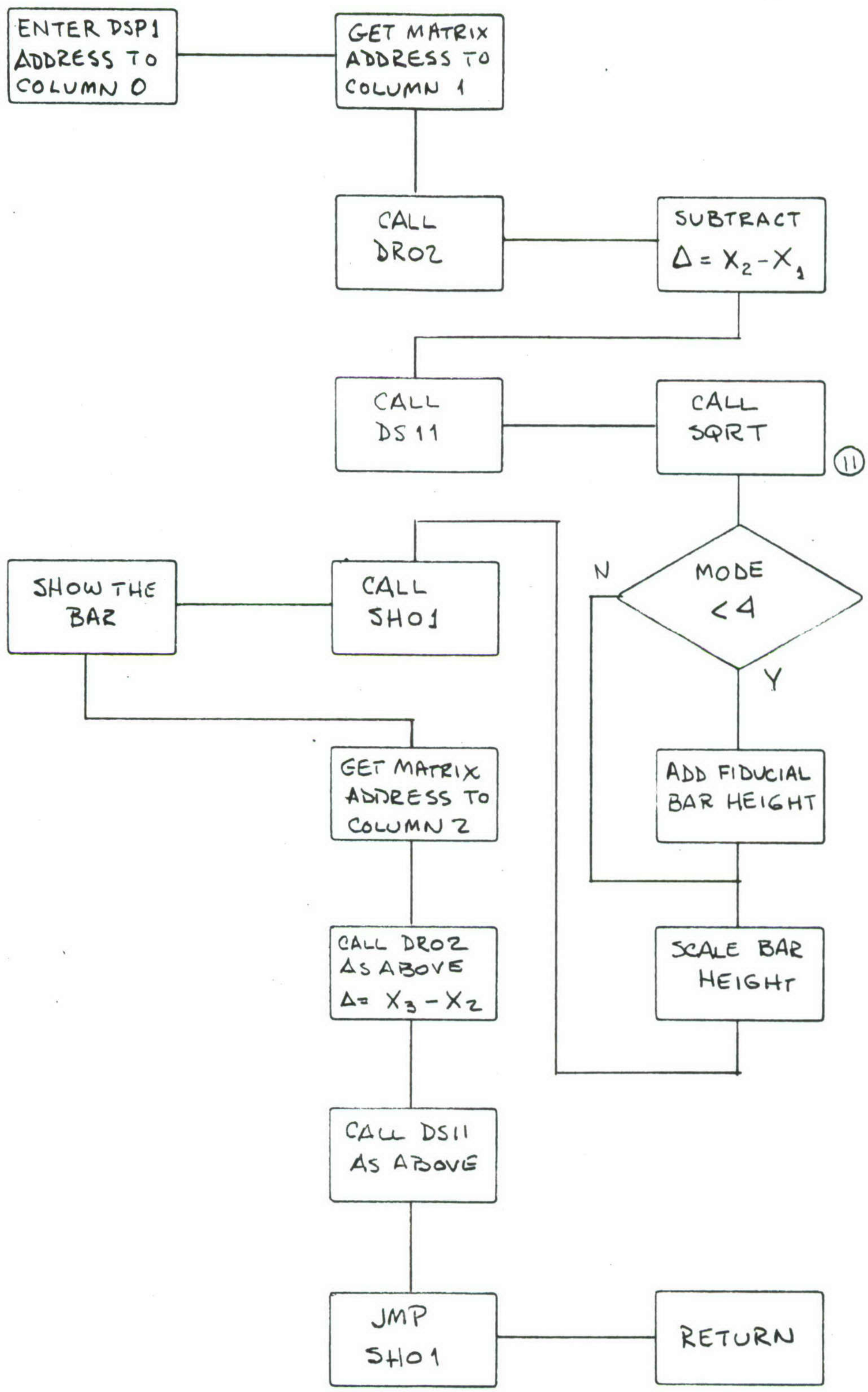
ENTER DRDB
CALL DR01
GET T.C.
GET SCALED DATA (FOUR BYTES)
STORE ON COLUMNS 0,2
CALL EXPF
10
EXPF STORES PROCESSED DATA TO COL 1
SET MATRIX ADDRESS
CALL EXPF
10
EXPF STORES PROCESSED DATA TO COL 3
RETURN

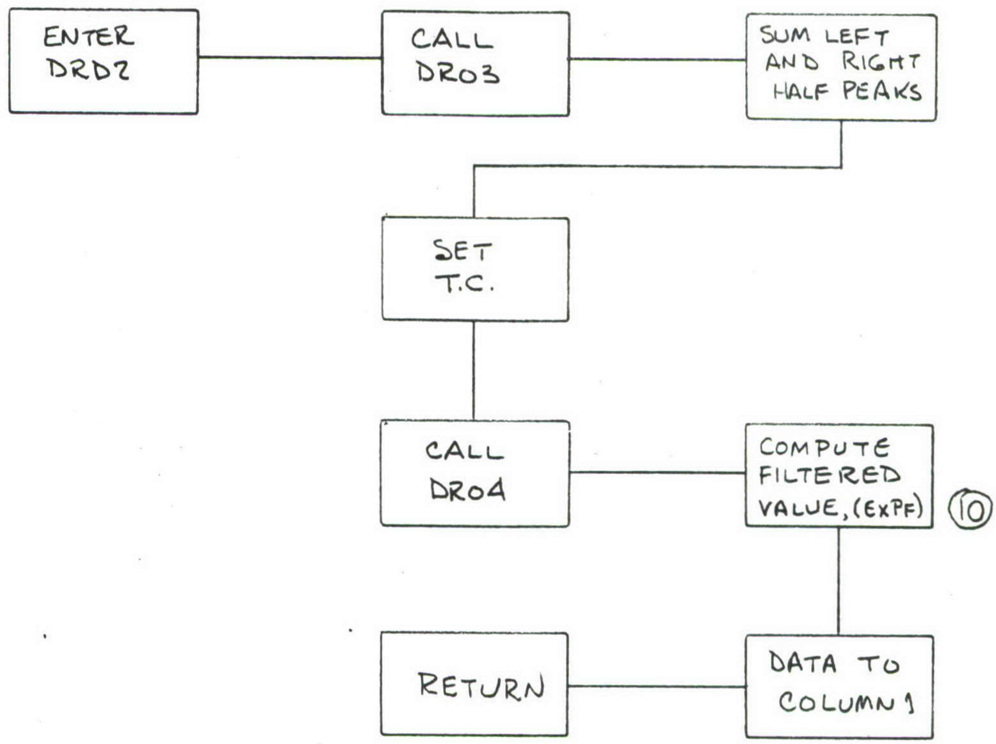
© DSPB



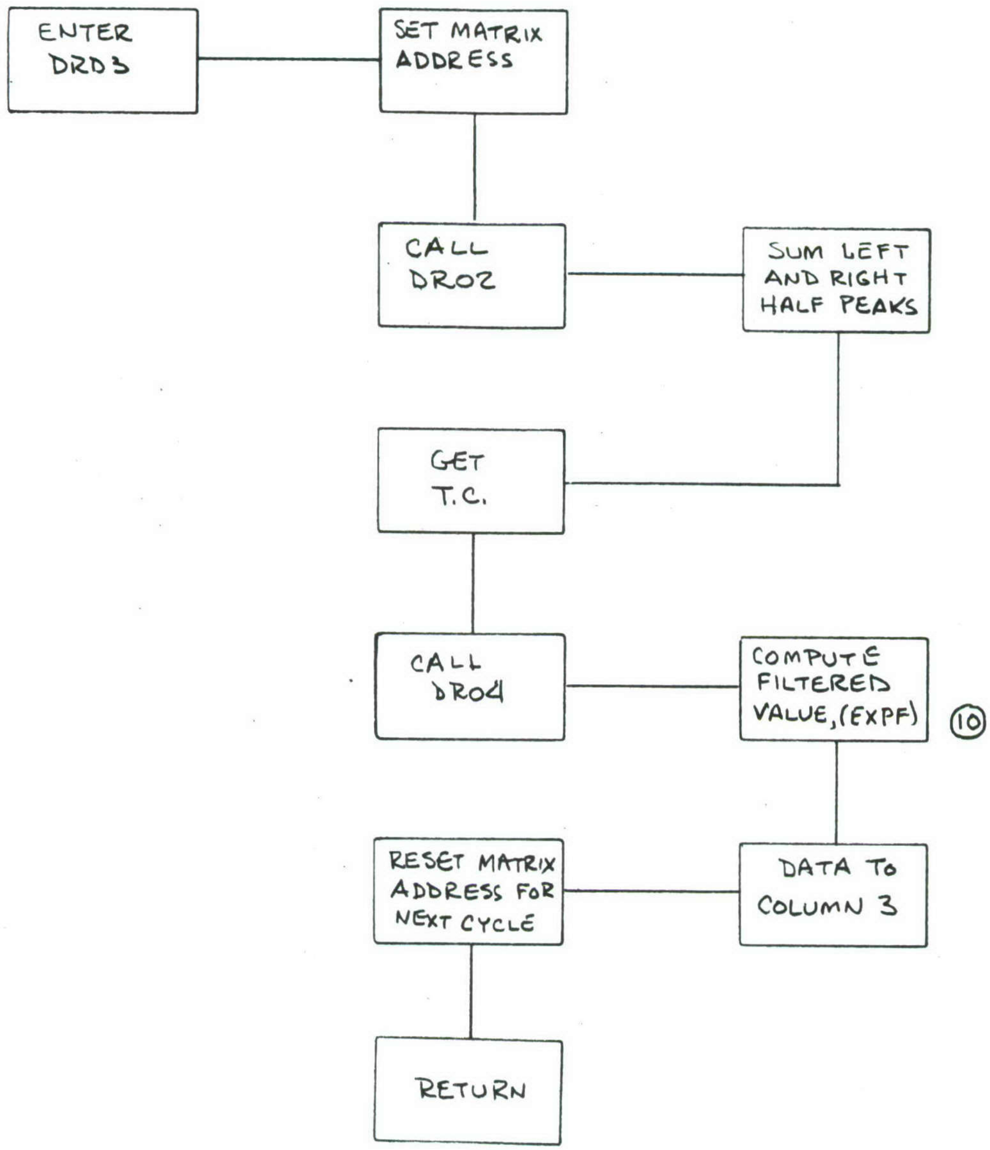
ENTER DSPB
GET MATRIX ADDRESS COLUMN 1
CALL SQRT
11
SQRT COMPRESSES DATA
GET MATRIX ADDRESS COLUMN 3
CALL SHOW TO LEFT BAR
SHOW THE BAR
CALL SQRT
11
SQURT COMPRESSES DATA
RESTORE MATRIX ADDRESS
SHOW RIGHT HAND BAR
RETURN


ENTER DRD1
CALL DR03
SUM LEFT AND RIGHT HALF PEAKS
SET T.C.
CALL DR04
COMPUTE FILTERED VALUE, (EXPF)
SET T.C.
DATA TO COLUMN 1
CALL DR04
COMPUTE FILTERED VALUE, (EXPF)
SET T.C.
DATA TO COLUMN 2
CALL DR04
COMPUTE FILTERED VALUE, (EXPF)
RETURN
DATA TO COLUMN 3


ENTER DSP1 ADDRESS TO COLUMN 0
GET MATRIX ADDRESS TO COLUMN 1
CALL DRO2
SUBTRACT $\Delta = X_2 - X_1$
CALL DS11
CALL SQRT
11
MODE < 4
N
Y
ADD FIDUCIAL BAR HEIGHT
SCALE BAR HEIGHT
CALL SHO1
SHOW THE BAR
GET MATRIX ADDRESS TO COLUMN 2
CALL DRO2 AS ABOVE $\Delta = X_3 - X_2$
CALL DS11 AS ABOVE
JMP SHO1
RETURN


ENTER DRD2
CALL DR03
SUM LEFT AND RIGHT HALF PEAKS
SET T.C.
CALL DR04
COMPUTE FILTERED VALUE, (EXPF)
10
DATA TO COLUMN 1
RETURN

(G) DRD3



ENTER DRD3
SET MATRIX ADDRESS
CALL DR02
SUM LEFT AND RIGHT HALF PEAKS
GET T.C.
CALL DR04
COMPUTE FILTERED VALUE, (EXPF)
10
DATA TO COLUMN 3
RESET MATRIX ADDRESS FOR NEXT CYCLE
RETURN

SUBROUTINE CALL LIST

CALL	ADDRESS	TITLE
TNON	1400	START ENTRY
PLOP	1420	PRIMARY LOOP
ENTR	1515	ENTER SPEC CALL
JEEX	1540	COMPARISON PROGRAM EXEC
EXIT	1546	CLEAR, RETURN PLOP
JENZ	1554	COMPARISON PROGRAM POINTER
SK01	1566	SKIP
CAB1	1625	CALB LOOP
CALB	1637	MANUAL CALIBRATE
CAB3	1650	
GTBL	1704	GENERATE TABLE
CAB2	1730	
DEC1	1770	DECREMENT CORRECTION CONSTANT
CALA	1775	AUTO CALIBRATE
DRD0	2002	CALA DATA REDUCTION
DECC	2077	DECREMENT CORRECTION CONSTANT
SQRT	2162	SQUARE ROOT ROUTINE
BL00	2156	KEEP SIGN, COUNT BITS
BL01	2171	LOOP FOR BLOO
BL02	2206	BIT COUNT MINUS 1
DRDB	2224	DATA REDUCTION FOR CALB
DR01	2242	UTILITY, DRED
EXPF	2273	SMOOTHING ROUTINE
EXP1	2377	RESTORE ADDRESS, DATA
DR02	2442	DIFFERENCE RIGHT AND LEFT HALF PEAKS
MADD	2465	MATRIX ADDRESS DIRECTOR
MAD1	2467	
MAD2	2471	
MAD3	2473	
MAD4	2475	
3SL1	2503	LEFT SHIFT ONE BIT

SUBROUTINE CALL LIST

CALL	ADDRESS	TITLE
3ASL	2525	LEFT SHIFT TO COUNT ≤ 16 BITS
3SR1	2532	RIGHT SHIFT ONE BIT
2ASR	2540	RIGHT SHIFT (2 REGISTERS) ONE BIT
3ASR	2556	RIGHT SHIFT TO COUNT ≤ 16 BITS
DR00	2563	RATIONALIZE, SCALE DATA
FLOD	2661	OVERRANGE ROUTINE
DSCL	2666	SCALE AND DISTRIBUTE DATA
SPEC	2715	SPECTROMETER ROUTINE
SPC1	2737	LOOP POINT, SPEC
SPC2	2764	SET UP DAC
SK02	3033	SKIP
SPC4	3066	TEST TABLE END
SPC3	3112	COMMAND SPECTROMETER
SERV	3144	ADDRESS, DATA SERVICE
SER3	3157	
DATA	3173	GET SPECTROMETER DATA
LINT	3213	LINEAR INTERPOLATION
LIN1	3217	LINT SEARCH LOOP
LIN2	3230	COMPUTE LINT
PRIM	3313	CLEAR TABLES
PRM1	3335	
PR11	3337	SET FULL DISPLAY
LDVR	3353	SET UP PROGRAM VECTORS
XMUL	3455	MULTIPLIER 8 X 16 BITS
XMU2	3467	
XDIV	3520	DIVIDER 24 ÷ 8 BITS
XDV2	3533	
MDOP	3572	MULTIPLY / DIVIDE LOADER
XDSU	3617	DOUBLE PRECISION SIGNED SUBTRACTION
PAD3	3626	TRIPLE PRECISION SIGNED ADDITION
PAD2	3636	DOUBLE PRECISION SIGNED ADDITION

SUBROUTINE CALL LIST

CALL	ADDRESS	TITLE
SKP2	3637	SKIP
SSIG	3647	SPECIAL SIGN ROUTINE
SSG1	3663	
SIGN	3670	OPERAND SIGN ROUTINE
SGN1	3676	
CSM3	3726	CHANGE SIGN 3 BYTES
CSM2	3737	
SKP1	3740	SKIP
STOR	3750	SAVE REGISTERS
EST4	3754	SAVE REGISTERS, EXTERNAL ADDRESS
EST3	3756	
EST2	3760	
REST	3764	RESTORE REGISTERS
RST4	3770	RESTORE REGISTERS, EXTERNAL ADDRESS
RST3	3772	
RST2	3774	
RESW	4000	READ SWITCHES, STORE
ZERO	4023	ZERO COUNTED LOCATIONS IN RAM
DSPB	4033	DISPLAY
SHOW	4061	SHOW A BAR
SHO1	4070	
DRD1	4077	DATA REDUCTION PROGRAMMED MASS
DRO4	4125	SMOOTH DATA
DRO3	4140	DATA DIFFERENCES
DSP1	4172	SET UP DISPLAY, PROGRAMMED MASS
DS11	4225	
DS1S	4255	
DRD2	4270	COMPARISON PROGRAM, FIRST PEAK
DRD3	4302	COMPARISON PROGRAM, SECOND PEAK
DSPO	4331	SKIP DISPLAY, (ONE WORD SUBROUTINE)
HCMD	4332	DOUBLE SWITCH SUPERVISOR

SUBROUTINE CALL LIST

CALL	ADDRESS	TITLE
HC00	4343	SELECTION 7-7 SET UP
HC01	4364	FIND NEW MASS RANGE
MTBL	4426	MAKE UP TABLE
HC04	4437	CLEAR MATRIX
HC02	4445	DOUBLE SWITCH MODE CHECK
HC06	4464	SET POINTERS
HC05	4505	TO SPEC
HC03	4524	ESCAPE TEST
SCAN	4544	SELECTION 7-6 SETUP
SCN1	4546	SEQUENCE VERIFICATION AND DISPLAY
SCN2	4551	SEQUENCE VERIFICATION AND DISPLAY
SCN3	4561	FIND NEW MASS RANGE
SCN7	4606	DOUBLE SWITCH MODE TEST WITH ESCAPE
SCN4	4636	START MASS AND SWEEP WIDTH
SCN5	4657	SWEEP SPECTROMETER
SCN6	4663	LOOP SWEEP STEPS
SCN8	4674	TIMER
PAT1	3370	REGISTER OVERFLOW STOP

ADDRESS	ITEM
3410	SYNTHETIC CALIBRATION MARKER MASS 12
3411	CM 1 MASS 36
3412	CM 2 MASS 90
3413	CM 3 MASS 206
3414	CM 4 MASS 264
3415	SYNTHETIC CALIBRATION MARKER MASS 340
3416	CALA TABLE LENGTH
3417	CALA NUMBER OF PEAKS
3420	CALA FIRST PEAK
3421	FIRST PEAK SOFTWARE GAIN
↓	
3427	FOURTH PEAK SOFTWARE GAIN
3430	CALB BASE, PROGRAM 0
3431	SOFTWARE GAIN
↓	
3436	CALB BASE PROGRAM 3
3437	SOFTWARE GAIN
3440	EXPONENTIAL TIME CONSTANTS (PAIRS)
↓	
3445	

ADDRESS	ITEM
10000	SERIAL COUNTER
10001	NEW MODE
10002	NEW PROGRAM
10003	OLD PROGRAM
10004	OLD MODE
10005	OLD START MASS (DOUBLE SWITCH)
10010	SYNTHETIC CORRECTION CONSTANT
10011	CC 1
10012	CC 2
10013	CC 3
10014	CC 4
10015	SYNTHETIC CORRECTION CONSTANT
10016	SAVE INDEX FOR LINT
10020	104
10021	V_1 LO
10022	V_1 HI
10024	104
10025	V_2 LO
10026	V_2 HI
10040	ARITHMETIC WORKING STORAGE
↓	
10051	
10060	REGISTER STORAGE
↓	
10064	
10066	SERVICE STORAGE
↓	
10072	

ADDRESS	ITEM
10160	TABLE CONSTANT AND TEMPORARY DATA
	STORAGE
10175	
10176	EXPONENT 2
10177	EXPONENT 3
10200	DATA MATRIX
	COLUMN 0
10237	
10240	
	COLUMN 1
10277	
10300	
	COLUMN 2
10337	
10340	
	COLUMN 3
10377	
10400	DATA DIFFERENCE (RESIDUES)
	COLUMN 4
10437	
10440	
	COLUMN 5
10477	
10500	
	COLUMN 6
10537	
10540	
	COLUMN 7
10577	
10742	INTERNALLY GENERATED MASS TABLE
10777	

PROGRAMMED MASS TABLE

PROGRAM	MASSES	MATERIAL
0	39	N-HEXANE
	41	
	43	
	57	
	86	
1	91	TOLUENE
	92	
	65	
2	93	NITROBENZENE
	65	
	30	
3	117	CCl_4
	119	
	121	
	82	
	47	
	166	C_2Cl_4
	129	
	59	
	94	
	96	
4	72	C_6H_6
	52	
	51	
	77	

	PROGRAM	MASSES	MATERIAL
	5	53	MNT
		54	
		77	
		106	
		107	
	6	128	NAPTHALENE
		127	
		129	
		64	
		51	
	7	119	DIETHYL BENZENE
		134	
		105	

MODE	PROGRAM	MASS RANGE
1	0	10 - 24
1	1	24 - 38
1	2	38 - 52
1	3	52 - 66
1	4	66 - 80
1	5	80 - 94
1	6	94 - 108
1	7	108 - 122
2	0	122 - 136
2	1	136 - 150
2	2	150 - 164
2	3	164 - 178
2	4	178 - 192
2	5	192 - 206
2	6	206 - 220
2	7	220 - 234
3	0	234 - 248
3	1	248 - 262
3	2	262 - 276
3	3	276 - 290
3	4	290 - 304
3	5	304 - 318
3	6	318 - 332
3	7	332 - 346

VI CONCLUSIONS AND RECOMMENDATIONS

The portable mass spectrometer system has demonstrated that part per billion detection performance can be available in a truly portable way. Although only the briefest of tests were possible due to a requirement for immediate delivery, the system was able to detect the lower boiling point solvents with a sensitivity comparable to prior vapor detection equipment which it resembles. The operation of the microcomputer and digital system meets all of the expectations, and, where new software may be desired it has the flexibility to be reprogrammed to suit such applications needs as may later be required.

Logistics of transportation are relatively simple. For transport, the equipment is furnished with easily procured batteries which will supply the high vacuum needs for a period of up to 48 hours. Power for this purpose may also be introduced via an external plug through a closed case. The cases are moderately heavy but manageable. The electronics and control section in its case weighs about 40 lbs, while the spectrometer case weighs just over 80 pounds. The cases are of moderate size, each measuring 26 x 18 x 9 inches. Supply at the destination requires less than 350 watts of commercial power from 110V 60Hz lines.

In view of the limited level of operating experience, it is recommended that a small support program using manufacturer's personnel and facilities in conjunction with Army project personnel be instituted.

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